

INSTRUCTION MANUAL

DATA TEK™ 9600

DTS-1 SERIES

OCTOBER 1975

ATLANTIC RESEARCH CORPORATION

TELEPRODUCTS

ALEXANDRIA, VIRGINIA 22314

TM 833

INSTRUCTION MANUAL

DATA-TEK™ 9600

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Manufactured by:

ATLANTIC RESEARCH CORPORATION

Teleproducts

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SECTION I

GENERAL DESCRIPTION

The DATA-TEK DTS-1 is a highly versatile test instrument for both ON-LINE system diagnostics as well as OFF-LINE diagnostics of both the terminal and the communication facility. Maximum flexibility is achieved by providing a versatile interface for EIA (RS-232) or MIL 188, neutral loop (wet or dry), and logic signals. The transmitter and receiver circuits are completely independent, permitting full duplex, loop back, end-to-end measurements compatible with other equipment already in the field.

The DATA-TEK may be operated in three basic modes. The MODE switch in the generator zone of the panel selects the function to be performed. Specific operation of various controls and indicators depends upon the test mode selected.

- DATA MODE: Generator and analyzer perform data- (e.g., character-) oriented functions such as sending ASCII code messages, measuring distortion, recognizing specific characters (called TRAP), and counting parity errors (CERT).
- 511/2047 MODE: Generator and analyzer operate in either of these standard bit patterns for BERT measurements (e.g., BIT or BLOCK error tests).
- LINE MODE: This mode is used principally for terminal/printer (alignment) tests whereby a variable length line from 1 to 159 characters is generated followed automatically by CR/LF.

1-1. General. The DTS-1 is 12.5 by 9.75 by 5.5 inches and weighs 11 pounds. Power is supplied to the DTS via an 8-foot AC power cord. Operating voltage is selected (internally) for 115 or 230 volts AC, 50/60 Hz. Accessories shipped with the DTS-1 are three small single-wire patch cords (internal-to-case) and one manual. The DTS-1 is designed to operate properly over a temperature range of +40 to +120°F and a relative humidity of 20 to 95 percent without condensation.

Table 1-1 lists the specifications for the input and output signals for the DTS-1.

1-2. Model Numbers. The model numbers assigned to the DATA-TEK 9600 series are:

DTS-1-1 Standard Catalog (suitcase) Unit
 DTS-1-2 Rack Mounting Unit
 DTS-1-3 Custom Unit
 DTS-1-4 Custom Unit

Table 1-1. Specifications.

Input	Data Signal Interface	
EIA	Monitor terminal pin 2, monitor modem pin 3. Threshold for marking is $> +1.3$ volts. Input impedance ≈ 27 kilohms. Input impedance 120 ohms resistive plus 1.5 volts drop. Optically isolated from ground. Input switching threshold fixed at 1/2 current and polar switches near ground $\approx \pm 3$ mA. TTL logic signal. DTS provides 2.2 kilohms load to +5 volts. External keyer must sink 2.5 mA to ground.	
LOOP		
TTL		
Output		
EIA		
LOOP	Pin 2 and pin 3 have separate drivers. ± 11 volts with current limiting at 10 or 20 mA. Rise and Fall times ≈ 10 microseconds linear symmetrical ramp. Dry keyer is solid state. Drops ≈ 3 volts. Polarity insensitive. Internal series 10 ohms 1/4-watt resistor for loop fuse. Wet keyer contains keyed constant current source. Polarity dependent. Internal supply of 100 volts can be adjusted to regulated external current from 20 to 65 mA. Regulation is maintained with 0 external resistance to a maximum external loop drop of 90 volts.	
Input	Pin	Auxiliary Interface
$\pm 3V$	1	Input resistance > 120 kilohms.
$\pm VM$	2,3	Input resistance 25 kilohms.
RESET	4	Input resistance 100 kilohms, switch point +2.5 volts.
STEP	5	Input resistance 100 kilohms, switch point +2.5 volts.
ISOC	6	Input resistance 3 kilohms, switch point +1 volt.
TTL	7	1 each, TTL input. Requires external 1.6 mA current sink to GND.
EXT	8	Input resistance 3 kilohms, switch point +1 volt.

Table 1-1. Specifications. (Cont'd)

Output	Pin	Auxiliary Interface
$\pm 12V$	16,15	± 12 volts sourced through series 1 kilohm.
IDLE	14	Internal source 2.2 kilohms to +5 volts. Will sink external load to +5 volts at up to 10 mA.
ERROR	13	Same as IDLE.
CLOCK	12	± 12 volts signal RS-232 compatible. Current limited to 10 or 20 mA. Rise and fall times are 10 microseconds (linear ramp).
TRAP	11	Same as IDLE.
TTL	10	Same as IDLE.
GND	9	Circuit ground for RS-232 pin 7 and logic.

1-3. Self-Test. Self-test capability is incorporated into all functions performed by the DTS-1. The Maintenance Section describes procedures by which all functions of the DTS may be verified by front panel self-test operations.

1-4. Output. Output signals are of five types:

- Four panel-selected data characters (distortion selectable).
- Four FOX messages of 64 characters (distortion selectable).
- Reversals (nondistorted).
- 511, 2047 bit patterns (nondistorted) conforming to CCITT standards.
- Up to 159 characters per line, plus automatic CR, LF.

1-5. Input. Input signals may be analyzed in several ways.

- MARK and SPACE Bias.
- PEAK TOTAL Distortion (includes effects of speed error, end, etc.).
- CERT: Parity error count.
- BERT: Bit error count in 511, 2047 patterns.
- BERT: Block error count in 511, 2047 patterns.

- ± 3 volts RS-232 threshold.
- 0 to 25 volts measurement on control leads.
- 0 to 100 mA measurement on loops.
- Detect (TRAP) presence of specific data character.
- Display data character bits.
- Polarity inversion for MARK and SPACE.

1-6. Interface. A versatile interface is provided to enable use with the following types of signals encountered in the field.

- RS-232 ± 12 volts.
- MIL-188 ± 12 volts (± 6 volts special order).
- Dry loop input (20 or 60 mA POLAR).
- Dry loop output.
- Wet loop output 20 or 60 mA at 100 volts (neutral).
- Loop supply with 3 multiple jacks in series.
- TTL (Mark = 1).
- TTL (Mark = 0).
- ± 12 -volt source (10 mA).

1-7. Data Formats. These data formats experienced in maintenance situations may be tested.

- Speeds to 9600 bits per second.
- Async data generator.
- ISOC data generator (at 21 internal speeds, plus two custom speeds).
- 511, 2047 patterns clocked from modem.
- 511, 2047 patterns internally clocked and clock derived by analyzer from received data.
- Async data monitor and character trap.
- Measured distortion on async and sync.

- Speed error (on non 1.5 stop codes).
- 5-, 6-, 7-, 8-level signals having 1, 2 stop elements.

1-8. Auxiliary Connector. An auxiliary connector has been provided for access to important internal signals to facilitate special test setups such as adding time delays, automatic polling with verification of response characters, etc. A series of applique modules is available for these special conditions to further enhance the value of the DTS-1.

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SECTION II

INSTALLATION

The standard DATA-TEK 9600 is delivered ready for use on 115 volts AC, 50/60 Hz.

- a. Plug the power cord into a 115-volt AC outlet.
- b. Turn the instrument on using the switch located in the upper right of the front panel labeled PWR OFF.
- c. Refer to Section III for detailed operating instructions. Refer to Section V for use of internal self-tests for performance verification.

The DTS-1-2, rack-mount unit, is factory-built with a 19-inch panel for standard 8.75-inch high RETMA mounting. All front panel connector-access to EIA and LOOP is maintained. Additionally, rear access is provided via duplicate EIA connectors, plus a 6-terminal barrier strip for remote LOOP IN and LOOP OUT jacks. Two additional wires must be connected to remote the loop mA meter capability. See Figure 2-1.

EIA connections may be remoted by using extension EIA cables.

LOOP OUT connection may be remoted by using series normal through jacks.

LOOP IN connection may be remoted by using tip-sleeve jack; however, an insulated Form A contact is required on the remoted LOOP IN jack to permit loop mA meter measurements.

NOTE

If LOOP OUT IS *not* remoted, a jumper must be placed between terminals 1 and 2 of the rear terminal strip.

Do not connect to front panel and rear (remoted) connectors simultaneously.

Do not apply EIA and LOOP signals simultaneously.

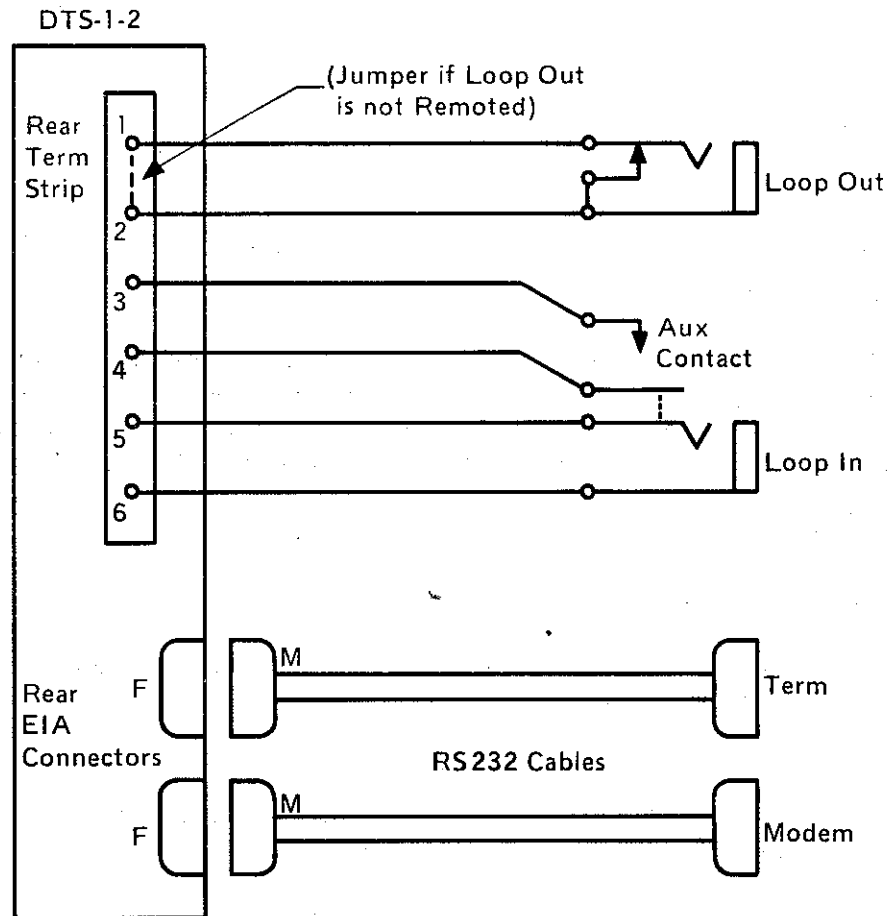


Figure 2-1. Remote Connections.

SECTION III

OPERATION

3-1. Controls and Indicators. Figures and Tables 3-1 through 3-7 identify the zones, controls and indicators used in the operation of the DTS-1.

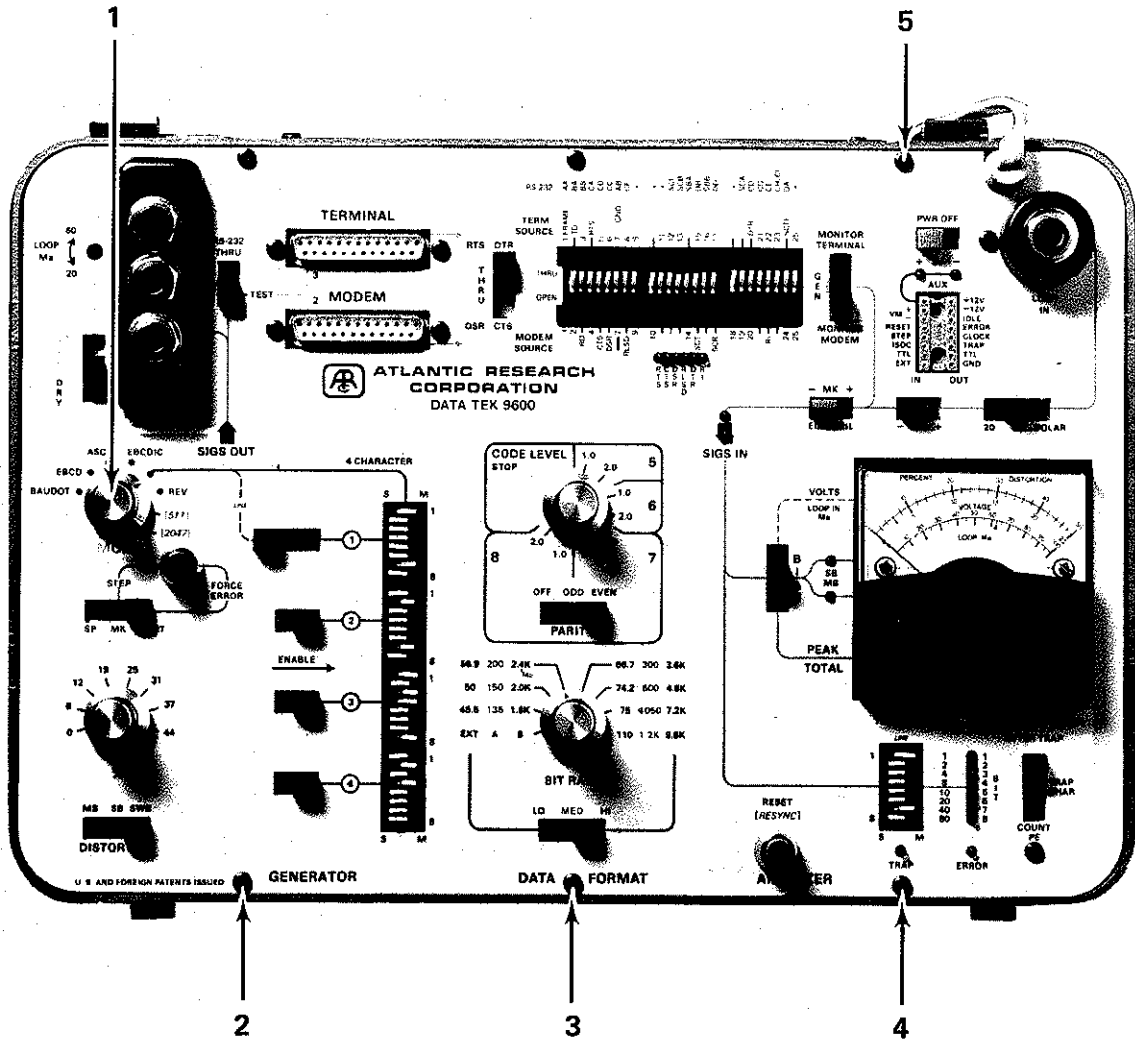


Figure 3-1. Panel Zones.

Table 3-1. Panel Zones.

Key	Control	Function
1	MODE SWITCH	This switch with the LINE switch determines the major functional characteristics of the DTS. The three modes are: • DATA Mode • LINE Mode • 511-2047 Mode
2	GENERATOR ZONE	All controls in this section of the panel affect the characteristics of the generated signal.
3	DATA FORMAT ZONE	These controls are common to the generator and analyzer.
4	ANALYZER ZONE	The analyzer operation is influenced by the MODE selection.
5	INTERFACE ZONE	This area of the panel is reserved for accessing the instrument through appropriate cables and patch cords.

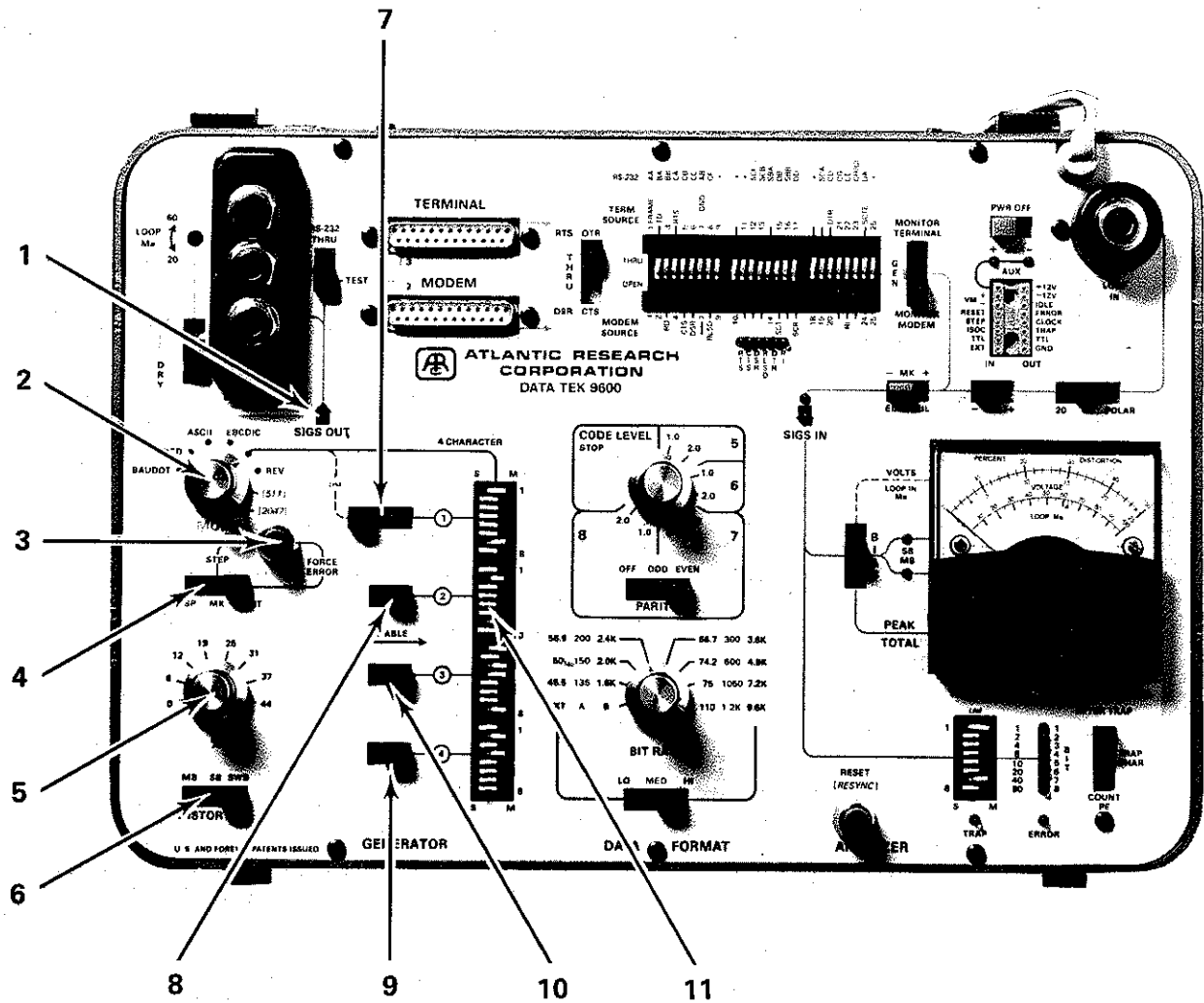


Figure 3-2. Generator.

Table 3-2. Generator.

Key	Control	Function
1	SIGS OUT Lamp	ON indicates space signals.
2	MODE	Selects the overall operational MODE of the DTS. a. DATA Mode ● Selects transmit messages in 4 codes, 4 characters, or reversals. ● Conditions analyzer to measure distortion, count PE, TRAP. b. 511-2047 Mode ● Selects bit pattern generated. ● Conditions analyzer to count bit block errors. ● Disables distortion meter. c. LINE Mode uses 4 Char Message ● Transmits up to 159 characters (by alternating char 1 and char 2) followed by CR/LF (using char 3 and char 4). ● Analyzer selects Line Length and Measure Distortion.
3	STEP/FORCE ERROR	a. DATA Mode ● STEP: Releases single message of 64 char or 4 char. ● Force error (continuous) inverts parity bit. b. 511-2047 Mode ● Step inoperative. ● Force error (continuous) inverts all data bits. c. LINE Mode ● Step -- Releases single line.

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3	STEP/FORCE ERROR	a. DATA Mode ● STEP: Releases single message of 64 char or 4 char. ● Force error (continuous) inverts parity bit. b. 511-2047 Mode ● Step inoperative. ● Force error (continuous) inverts all data bits. c. LINE Mode ● Step — Releases single line.

Table 3-2. Generator. (Cont'd)

Key	Control	Function
4	SP-MK-CONT	● FORCE ERROR (continuous) resets line counter for the next character and inverts parity for all characters while operated. Output signal is Idle Space (SP) or Idle Mark (MK) or continuous transmission for the 5 data messages. IDLE (MK) position enables STEP switch and CONT position enables Force Error.
5	%	Selects degree of distortion on the leading edge of each mark bit (Bias).
6	DISTORTION	Selects early transition Mark Bias (MB) or late transition Space Bias (GB) or alternates on character basis (SWB).
7	LINE (Char 1)	Selects LINE MODE for both generator and analyzer. 4 CHARACTER MODE must be selected.
8,9, 10		Enables characters 2,3,4. Disabled characters maintain the output idle mark for that character's time slot (including start pulse).
11		8-bit switches for each of 4 characters to be transmitted. Bits of higher order than the selected code level are ignored.

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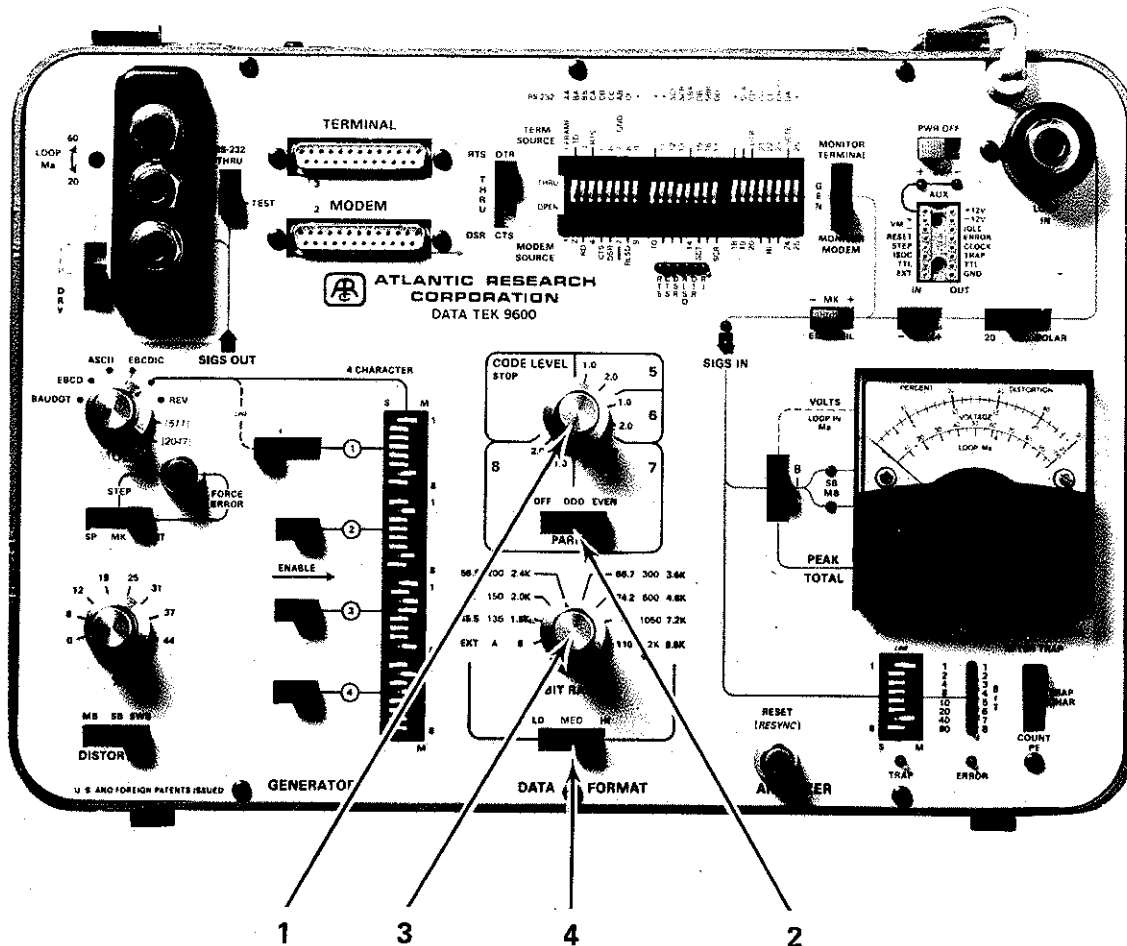


Figure 3-3. Data Format.

Table 3-3. Data Format.

Key	Control	Function
1	CODE LEVEL/STOP	Selects number of bits in each data character and number of stop bits.
2	PARITY	Determines use of parity bit on 7- and 8-level data characters. OFF position enables all BIT LEDs on the analyzer and all bit switches of the generator 4 characters. Error LED is disabled. EVEN/ODD positions enable the ERROR LED on the analyzer to display parity errors. TRAP character bit switches in analyzer must <i>select parity and higher order bits SPACE</i>. Parity is internally calculated and inserted into all transmitted characters (character bit switches for parity are ignored).
3	BIT RATE	Determines internal timing source for data characters and 511, 2047 patterns and external clock. External position depends upon the MODE switch. • Data Mode and LINE Mode: EXT position requires 128 X Baud input to the EXT pin of the AUX connector. • 511-2047 Mode: EXT position (Synchronous only) requires transmit clock (SCT) from modem into ISOC pin of the AUX connector for the generator and uses receive clock SCR from modem into EXT pin of AUX connector for the analyzer.
4	LO-MED-HI	Selects one of the three ranges of BIT RATE selector.

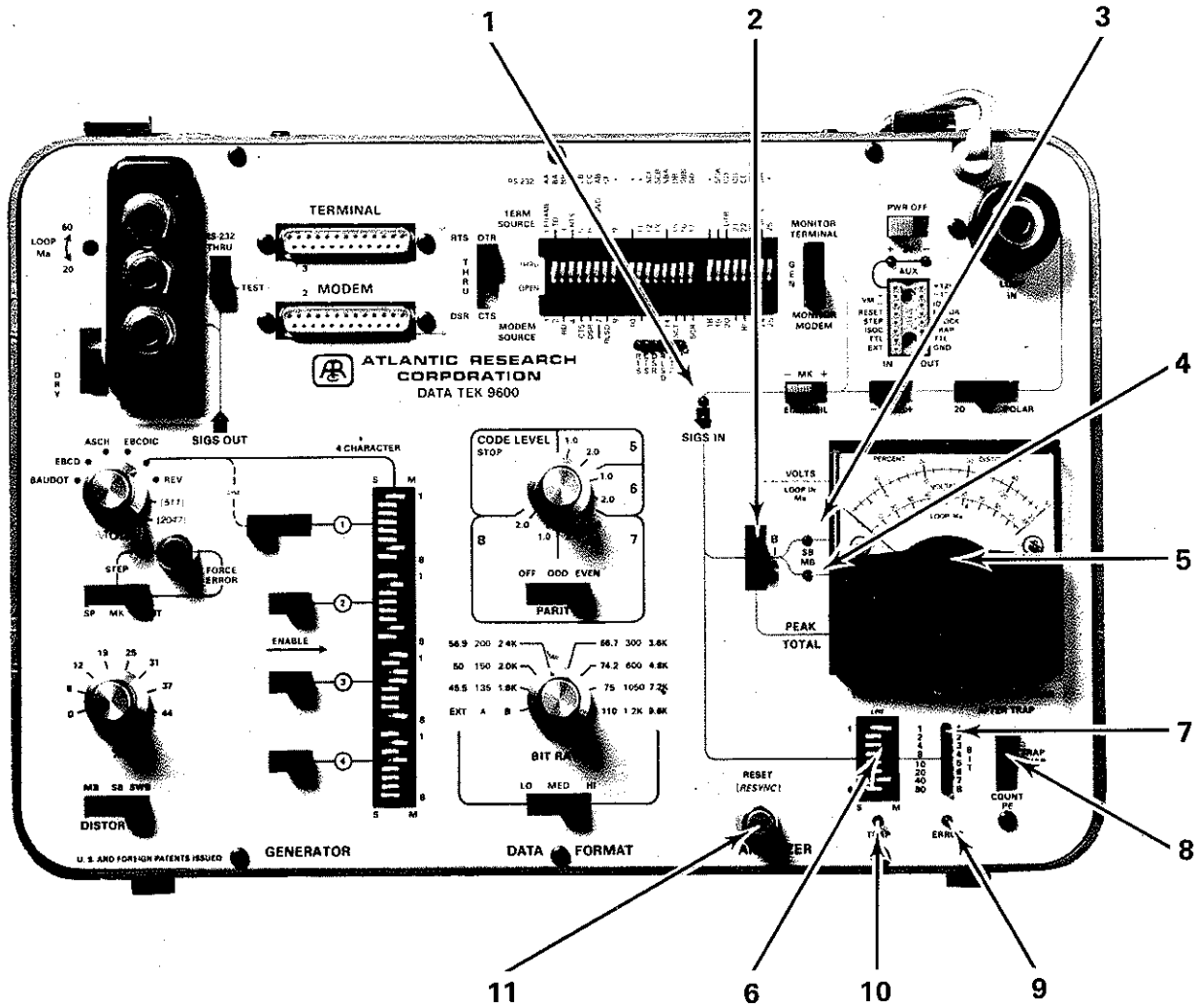


Figure 3-4. Analyzer

Table 3-4. Analyzer.

Key	Control	Function
1	SIGS IN Lamps	2 lamps: 1 inside arrow, ON for space; 1 outside, ON for MARK signal.
2	BIAS	Selects meter to read: 0 to 25 volts, 0 to 100 mA, or BIAS, PEAK TOTAL distortion. In PEAK TOTAL the meter will "pump" up and hold the maximum reading until Reset.
3,4	SB, MB Lamp	ON indicates Space Bias or Mark Bias of the input signal. One lamp is <i>a/ways</i> ON even in absence of data.
5	METER	Visual readout of volts, mA, percent distortion.
6	TRAP CHAR LINE Switches	Operates in 3 modes: 1. TRAP CHARACTER: Enter DATA BITS. When using Parity EVEN or ODD, the parity bit and higher bits must be Space. 2. LINE: Enter number of characters per line to be followed by CR/LF. 3. 511 and 2047 pattern errors: On Error count, enter number of errors tolerated before alarm (e.g., threshold).
7	BIT Lamps 1-8	Operate in 3 modes: 1. Data Mode: Characters are displayed or count of Parity Errors. 2. LINE: Counts characters per line. 3. 511-2047: Counts errors, bits or blocks.
8	DISPLAY NEXT CHAR COUNT PE	Controls usage of TRAP bit switches and BIT lamps.
9	ERROR Lamp	Date Mode: Displays Parity Errors 511, 2047 Mode: Displays BIT Errors.
10	TRAP Lamp	Indicates character has been trapped, or END of line, or Error Count threshold.
11	RESET/RESYNC	Resets meter, trap lamp, resyncs 511, 2047 Pattern Receiver.

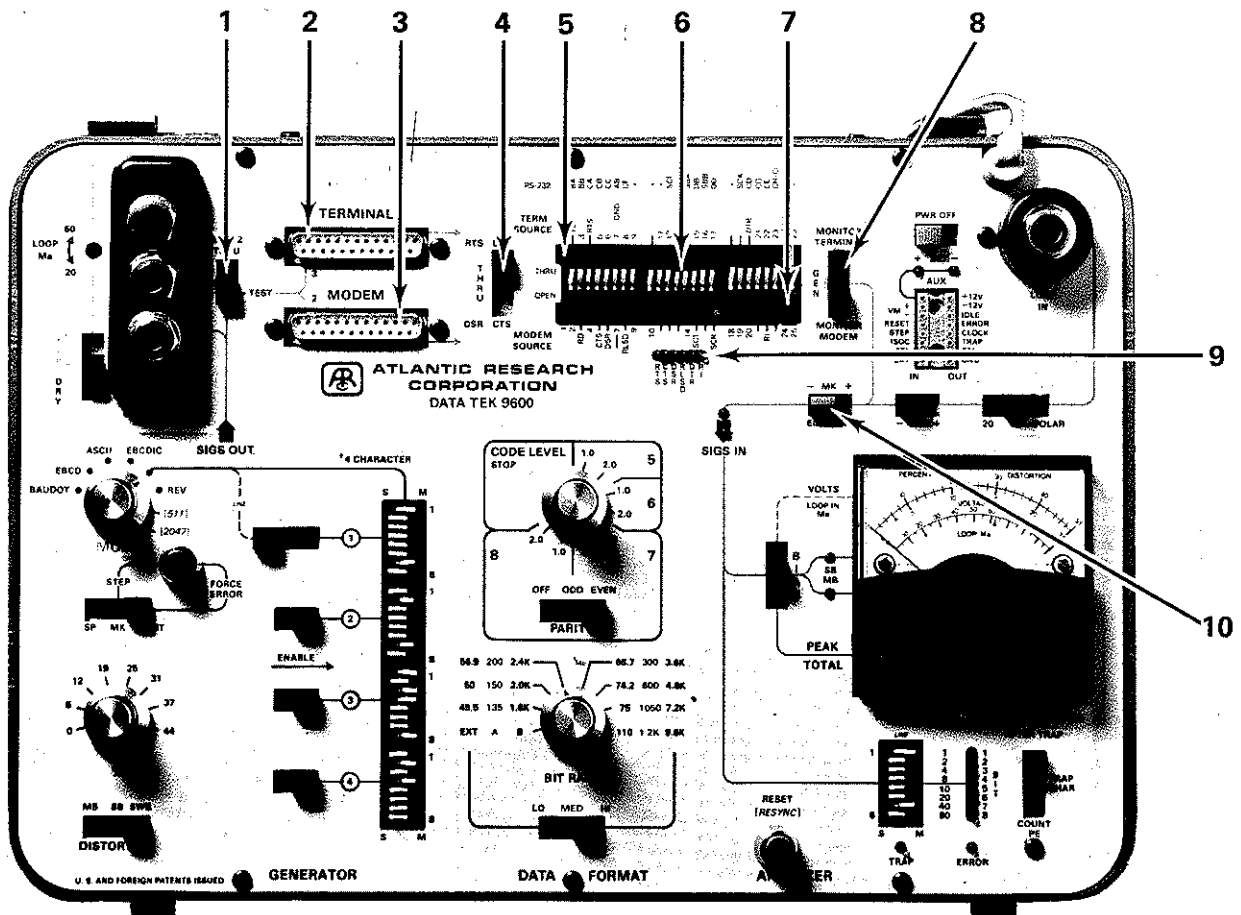


Figure 3-5. EIA Interface.

Table 3-5. EIA Interface.

Key	Control	Function
1	RS-232 + THRU	THRU: Metallic connection. Test position breaks pin 2, 3 paths between modem and terminal connectors and transmits SIGS OUT into terminal connector pin 3 and into modem connector pin 2.
2	TERMINAL	Connect to terminal or DTE.
3	MODEM	Connect to modem or DCE.
4	RTS/DTR – THRU – DSR/CTS	Metallic <i>thru</i> on indicated leads. Selected position breaks only the 2 leads shown and provides +12 on the output via 1K resistors.
5	TERM SOURCE	Row of 25 test points directly access the terminal connector.
6	THRU-OPEN Switches	Breaks the indicated EIA leads (except pin 7). Switches are directly connected to the terminal connector.
7	MODEM SOURCE	Row of 25 test points directly access the modem connector.
8	MONITOR TERMINAL – GEN – MONITOR MODEM	Selects source of EIA signals to analyzer. Input impedance is >27 kilohms.
9	6 Lamps	Monitor status of 6 indicated leads at the output of the DTS. ON equals positive >3 volts.
10	EIA MIL	Selects polarity of <i>input</i> and <i>output</i> signal as – or + marking for EIA and TTL signals. – is same as logic 0 (GRD) and + is logic 1 (POS).

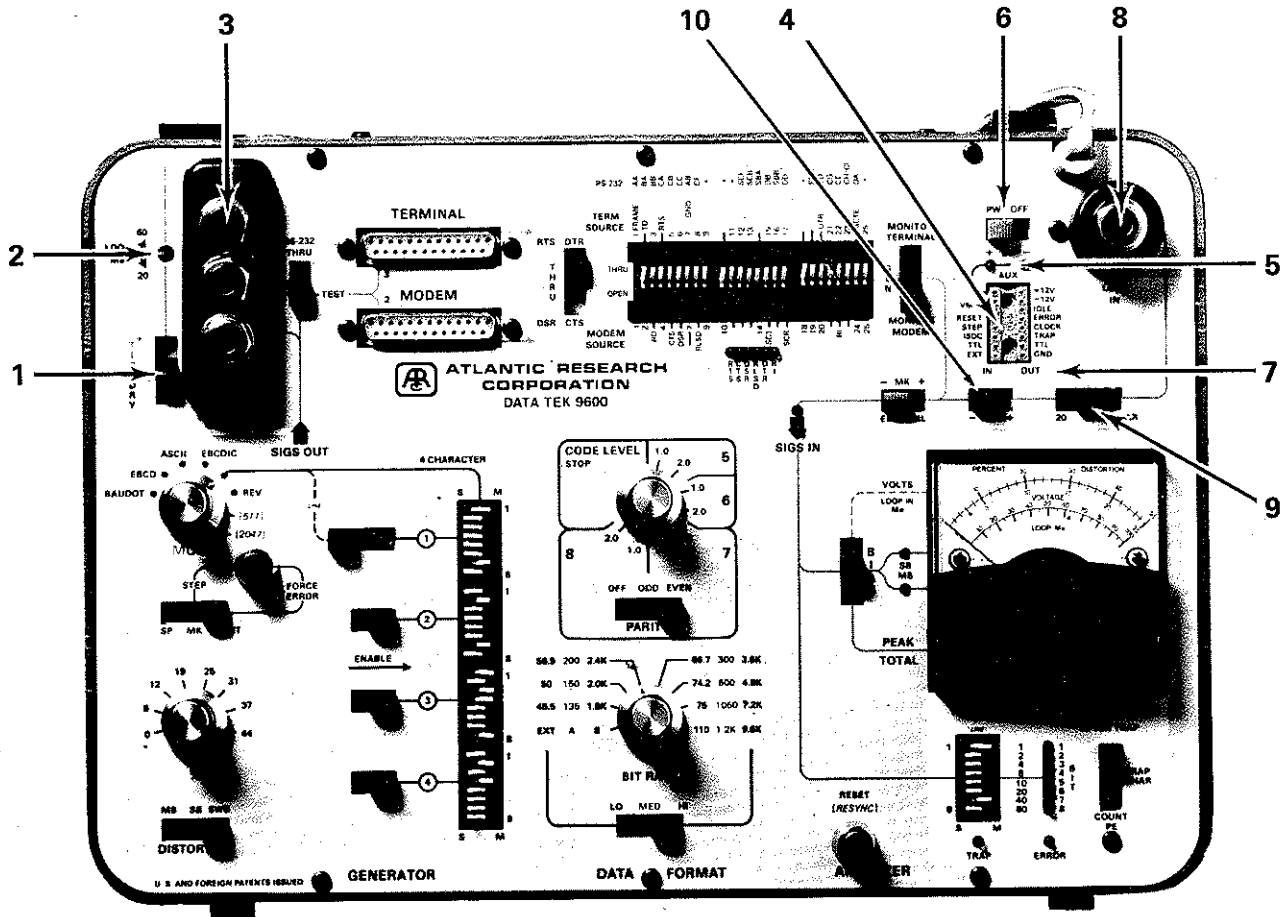


Figure 3-6. Loop Interface.

Table 3-6. Loop Interface.

Key	Control	Function
1	DRY/ $\pm$ TIP	Selects Dry keyer or internal 100-volt battery tip polarity.
2	LOOP mA	Adjustment of internal automatic current regulator from 20 or 60 mA. Regulation is maintained for external loop voltage drop from 0 volt (short) to 90 volts.
3	LOOP OUT	3 series tip sleeve jacks for loop output. Accepts standard WE347 or PJ055.
Key	Control	Function
4	AUX IN	Patch cord access for internal signals. $\pm 3V$ (1) 27 Kilohms input impedance voltage threshold indicators. $\pm V_m$ (2-3) Two patch cords access the 0- to 25-volt scale of the meter (selects VOLTS position). Input impedance is 25 kilohms. RESET (4) Positive logic input operates the RESET switch function. STEP (5) Positive logic input operates the STEP switch function and also resets TRAP light. ISOC (6) EIA level input from modem source test point for SCT. a. Data Mode: ISOChronous operation is achieved by generating data phase-correlated to the modem clock (when same bit rate is selected on panel). b. 511-2047 Mode: Synchronous operation only, select EXT bit rate and output signal is generated by using the modem clock. TTL (7) TTL logic level interface for data signals. EIA-MIL SW is used to select logic 0 (-) or 1 (+) for mark.

Table 3-6. Loop Interface. (Cont'd)

Key	Control	Function
4	AUX IN	EXT (8) EIA level input ($> \pm 3V$) for clocking. Controlled by EXT position of BIT RATE switch. In the DATA mode supply external oscillator having a frequency of 128 times the desired BIT RATE.
5	$\pm 3V$ Lamps	Threshold indicators for voltages $> +3$ volts or > -3 volts.
6	PWR OFF	AC power switch.
7	AUX OUT	Patch cord access for internal signals.
		+12V (16) +12 volts supplied through 1 kilohm.
		-12V (15) -12 volts supplied through 1 kilohm.
		IDLE (14) Positive logic signal after the generator completes sending a single STEP message.
		ERROR (13) Positive logic signal for each bit error or each parity error.
		CLOCK (12) EIA compatible ± 12 -volt clock signal derived from the generator.
		TRAP (11) Positive logic signal follows TRAP light.
		TTL (10) Logic signal follows generator data output. Polarity for MARK is selectable by the EIA/MIL switch.
		GND (9) Circuit ground. Also connected to EIA pin 7.
8	LOOP IN	Tip sleeve input loop jack. Accepts WE347 or PJ055.
9	20-60-POLAR	Selects input loop threshold switch point.
10	$\pm$ TIP	Selects tip polarity for LOOP IN jack.

Table 3-7. Internal Controls — Located on PC Board C.

Key	Control	Function
1	115-230 SW	Selects input voltage to power supply for 115 or 230 volts AC.
2	STRAP B (511-2047 Mode)	Position 1 conditions the counter to count BIT errors. Position 2 conditions the counter to count BLOCK errors. NOTE DDT-1-1, DTS-1-2, DTS-1-4 shipped strapped for block count. DTS-1-3 shipped strapped for bit count.
3	FUSE	1/4A SLOBLOW.

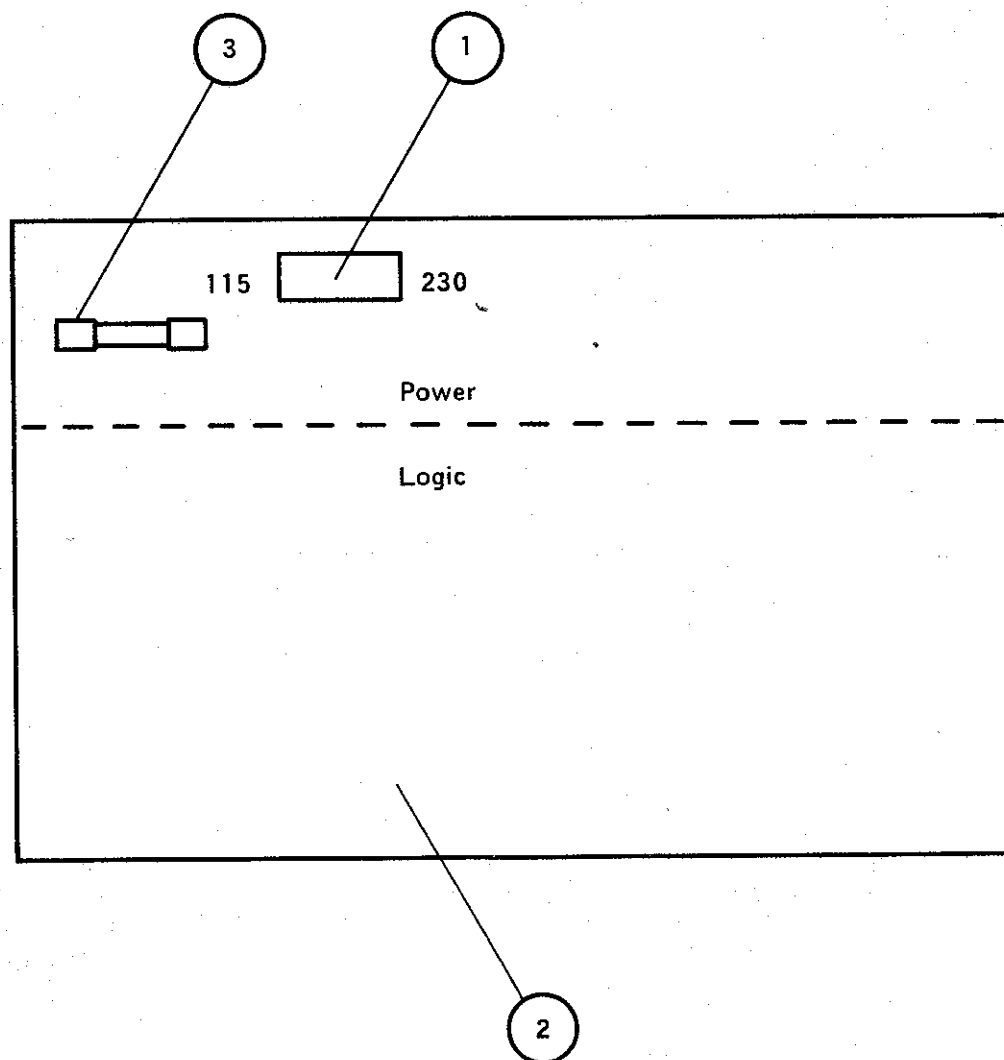


Figure 3-7. Internal Controls.

3-2. Applications. This section of the manual shows pictorially the positions for switches, cables, jumpers and readings for typical applications.

3-2-1. Signal Interface. The top zone of the front panel is reserved for the single interface, e.g., interconnecting the DTS into the circuit to be measured.

3-2-2. EIA ON-LINE Monitor. Figure 3-8 shows two methods for using the DTS to monitor signals ON-LINE. Figure 3-8a depicts the DTS in series with the signal path. Metallic-through connections are maintained between the modem and terminal within the DTM. Note that 3 switches must be set to THRU to obtain complete continuity.

Each of the EIA leads can now be opened (except pins 1, 7) and patched to +/- 12 volts.

"Transparency" is maintained by using a high impedance bridging amplifier (27 kilohms) to sample the EIA signals.

Figure 3-8b shows an application where there is already installed a bridging "T" adapter. In this case, none of the EIA leads can be opened or forced.

EIA OFF-LINE TESTS are accomplished according to the hook-up shown in Figure 3-9. Tests may be performed toward a MODEM or toward a TERMINAL.

Note that certain "thru" switches are now positioned for a TEST condition, thereby enabling the DTS to generate signals into the RS-232 interface.

LOOP ON-LINE MONITORING is simply shown in Figure 3-10a where an existing series monitor jack is available. The DTS places in series with an existing loop approximately 100 ohms plus 1.5 volts.

Where there is no series monitor jack, the 3 series MULT jacks on the generator can be used as shown in Figure 3-10b. The generator must be selected to Idle Mark (MK) and DRY output. The MULT jacks will present approximately a 2-volt drop due to the internal keyer.

Proper selection of + TIP or - TIP is determined by activity on the SIGS IN light. The correct loop current input must also be selected for a 20 mA, 60 mA neutral, or polar current loop.

Loop off-line tests are easily accommodated using the hook-up shown in Figure 3-10c.

If the loop under test has no battery, the DTS will supply a 100-volt regulated current. The correct TIP polarity must be selected.

IF ANY EXTERNAL BATTERY VOLTAGE IS PRESENT ON THE LOOP, DO NOT SELECT TIP + OR TIP - POSITIONS FOR LOOP OUT.

Adjustment of the output current can be performed by adjusting the small panel control and selecting LOOP IN mA for the ANALYZER meter.

If the Loop under test

- CONTAINS EXTERNAL BATTERY
- *AND CONTAINS MEANS FOR CURRENT ADJUSTMENT*

then select LOOP output DRY.

3-2-3. On-Line Measurements. A number of on-line measurements may be made with the DTS. The more prevalent are described in detail. On-line measurements are particularly useful because the system is actually analyzed under real operating conditions.

This section deals primarily with the ANALYZER section of the front panel.

EIA voltage measurements can be made by using two jumpers as shown in Figure 3-11a. The meter presents 25 kilohms across the circuit, thereby causing negligible loading while a measurement is being made.

Loop current levels are measured by using the 0 to 100 mA scale of the analyzer meter. The circuit connections shown in Figure 3-11b also indicate positions of $\pm$ TIP and LOOP-IN mA switches.

Distortion (DSTN) is measured only in the *DATA Mode* as shown in Figure 3-11c. TRAP or Count PE positions should normally be used. When the Display Next Character After Trap position is used and the character is displayed, the analyzer ceases measurement of DSTN.

BIAS or Peak Total can be selected. the MB, SB lights respond only to Mark and Space Bias in either position (Bias or Peak Total).

Character Trap is very useful to verify presence of certain control characters, address characters in a poll, etc. Figure 3-11d shows the TRAP bit switches selected to detect an ASCII "5." The lights continue to follow the bit patterns of the incoming data but the TRAP light will come ON when the character is TRAPPED.

Display Next Character After TRAP position causes the eight bit lights to latch and hold the character (and ignore any more input characters until the RESET switch is operated).

CERT is a Character Error Rate Test, otherwise known as a Character Parity Error Count. In the Data Mode, select the desired Parity Convention EVEN or ODD and the bit lights will count parity errors. Figure 3-11e shows a count of 52 parity errors.

The ERROR light will be ON for each character in error. Continuous errors will cause the light to remain ON.

3-2-4. Terminal Tests. These tests are shown generated directly into a terminal; however, the tests can just as well be generated into a modem link to a terminal, CPU, controller, etc.

This section deals primarily with the generator zone of the panel.

TEST MESSAGE GENERATION and DIST THRESHOLD are easily obtained as shown in Figure 3-12a. For example, an ASCII Message with 25 percent Space Bias is selected and the 4 characters are inhibited. The message will pause (MARK) for 4 characters, then send the 60 remaining characters in the message.

The analyzer is shown monitoring the GENERator so the meter will authenticate the amount of distortion actually generated.

As the % Distortion is increased, the terminal/printer can be observed for garbled copy.

Polling a terminal is extremely valuable with the DTS. This capability avoids reliance on CPU software and permits testing prior to circuit availability. Figure 3-12b shows selection of a 4-character poll "ABCD" in ASCII.

Verification of Keyboard Characters is a basic test of the terminal's transmit logic. Figure 3-12c shows the Analyzer Bit lights as they display receive data characters. ASCII "A" is shown.

Trap Answerback Characters is vital to any terminal test capability. Figure 3-12d shows the TRAP function of the DTS for a 2-character answerback of "AC." The trap light indicates the "A" was received and the Bit lights display the "C."

Automatic polling can be accomplished by using an applique module in the AUX connector to tie the TRAP signal to the STEP and reset input.

Manually operate the STEP switch to release the first poll, and when the answerback is trapped, the STEP will be electrically generated first Poll, and when the answerback is trapped, the STEP will be electrically generated to cause another Poll. 3-2-5. Printer Tests. The LINE mode is used for the printer tests. Both the analyzer and generator controls are used in this mode.

3-2-5. Printer Tests. The LINE mode is used for the printer tests. Both the analyzer and generator controls are used in this mode.

Figure 3-13 shows the mode LINE, and Trap/LINE Switch positions. The first 2 of the 4 characters are repeated 96 times (A1 A1 A1 A1) followed by character 3 (CR) and character 4 (LF). Selection of the number of characters per line is made by using the analyzer TRAP/LINE bit switches as shown. When the end of the line is reached, the trap light will blink ON. Operation may be in the continuous or stepped mode.

Variable length lines with automatic CR/LF are selected from 1 to 160 characters excluding CR/LF.

Line Overprint and Print Registration is achieved by disabling character 4(LF).

Print Head Return Time Delay can be tested by using an applique module in the AUX connector. The applique circuit simply incorporates a R-C delay from the last character transmitted (IDLE) to activate the STEP input. The cycle is repetitive and various RC delays can be used.

3-2-6. Tests into the Transmission Facility. The DTS provides an extremely versatile interface for the transmission facility.

Synchronous 511-2047 BERT test set-up is shown in Figure 3-14a. Two jumpers are used to bring the modem clock SCT into the generator (ISOC) and the SCR Clock into the Analyzer (EXT). The Speed Switch must also be on EXT.

BIT or BLOCK count is an internal strap inside the DTS. When the ERROR light is continuously ON, this usually indicates loss of Sync and manual Resync should be performed.

Asynchronous 511-2047 BERT test set-up is shown in Figure 3-14b. No jumpers are used since the DTS generator and analyzer bit rates are selected on the panel (1200). The Analyzer recovers clock from the received signal. Thereby an asynchronous (non-clocked) modem BERT measurement can be made.

ISOChronous Data Mode is essential for testing Character Error Rate CERT over digital data links. The jumper shown in Figure 3-14c uses the transmission link clock to phase correlate the output bit pattern of the generator. The front panel of the DTS must select the proper Bit Rate for the interface.

3-3. Functional Description. This section describes the basic functions of the major DTS elements.

3-3-1. DATA Generator. The data generator transmits data messages with the capability of introducing Marking and Spacing Bias. Four messages consist of 64 characters (Baudot, ASCII, EBCD, and EBCDIC are standard) and a fifth message of 4 characters. The first 4 characters of the 64-character messages are selected by the 4 characters' bit switches on the panel. The remaining 60 characters are permanently stored in a ROM chip. The message content is given in Section 4-10. Reversals are generated without distortion.

Distortion may be introduced into the signal by selecting Marking, Spacing or Switched Bias in 6 percent increments from 0 to 44 percent.

A single message can be released by the step switch or the message can be transmitted continuously. In continuous transmission, the STEP switch forces parity errors.

3-3-2. LINE MODE Generator. In the LINE mode, the 4-character message is altered by repeating characters 1 and 2 up to a 159-character line, then characters 3 and 4 are sent (should be programmed for CR/LF).

The TRAP bit switches on the analyzer select the number of characters per line (not including CR/LF). The balance of the analyzer circuits are inoperative (DSTN, etc.).

The BIT lights on the analyzer count each character in the line and the TRAP light will blink on at the end of the line.

The signal can be distorted with bias and released single line or continuously.

3-3-3. Data Analyzer. The analyzer performs four functions: Distortion Measurement, Speed Measurement, Character Verification, Character Parity Error Count.

Distortion is measured as Bias or Peak-Total with a resolution of 1.5 percent. Bias readings update the meter on every space-to-mark transition. MB and SB lights respond to early or late occurrences of this transition. One light will be ON. Peak-Total readings update the meter on every Mark-to-Space or Space-to-Mark transition but only when the new distortion exceeds the previous reading.

Speed error may be read by observing that the Peak-Total reading increases with code level. When the readings increase with code level, the actual percent speed error is obtained by dividing the percent distortion reading by the code level, e.g., 32 percent distortion at 8-level equals 4 percent speed error (distortion would also read 28 percent at 7-level, 24 percent at 6-level, 20 percent at 5-level). This measurement is applicable to any synchronous signal or continuous asynchronous signal having multiples of unit stop elements.

Character verification is performed in three ways:

- a. By observing the 8 bit lights on the analyzer. These display the received character until the next character updates the display.
- b. By selecting the bit pattern for the desired character in the TRAP switches. When the character is received, the TRAP light will come ON until manually reset.
- c. An *unknown* character may be easily determined by using the Display Character after the TRAP. The trap character readies the 8 bit lights to latch onto the next character and disregard any other received characters. The Bias reading is automatically reset; however, the Peak Total reading is recorded up to the selected character only and disregards higher distortion readings that may occur after the desired character is received.

3-3-4. DATA Format. This section of the DTS-1 controls the code structure of the Data Characters (code level, stop bits and parity convention) for the DATA and LINE modes.

The BIT RATE selection applies to all operational modes of the DTS-1. The EXT position permits synchronous operation of the 511-2047 mode for testing synchronous data sets.

All controls in the data format zone of the panel apply to the generator and analyzer.

3-3-5. 511-2047 Generator. In this mode the generator releases a continuous undistorted pattern complying with the CCITT and WECO convention for pseudo-random patterns. The pattern may be inverted to comply with a few non-standard analyzers by using the EIA-MIL switch.

Errors may be forced for the duration of the operation of the switch. Errors consist of inverting the bit pattern.

The generator operates at the selected bit rate. To test a synchronous modem, use the EXT position and patch the modem clock SCT (pin 15) to the ISOC pin of the AUX connector.

3-3-6. 511-2047 Analyzer. In this mode the analyzer generates its own independent pattern which is compared with the received pattern.

The RESET [RESYNC] switch is operated to manually sync the analyzer. When in sync, the ERROR light will be OFF. The ERROR light indicates each bit error, thus indicating the density of errors and hence if out of sync, the light will be predominantly ON.

An Error Count is displayed on the BIT lights on the analyzer (a maximum count of 159 errors). An internal strap selects the counter input as BIT or BLOCK errors. One or more BIT errors in a block constitutes one block error.

Preset error threshold alarm is provided by selecting the desired threshold count using the TRAP switches and observing when the TRAP LED comes ON.

For non-clocked modem tests, the analyzer operates on the selected bit rate and derives the proper clock phase from the received data.

For testing synchronous modems, patch the modem receive clock SCR (pin 17) to the EXT pin on the AUX connector and select the EXT position of the Bit Rate switch.

3-3-7. EIA Interface. The DTS-1 provides a metallic *through* path for all EIA leads. All leads (except 1 and 7) can be opened by using the switches on the panel. Four leads can be forced ON by a panel switch RTS/DTR and DSR/CTS. The signal leads pin 2 and 3 are opened in the TEST RS-232 mode and the output signal is applied to both the modem via pin 2 and the terminal via pin 3 (through separate drivers).

EIA output signals are current limited to 10 or 20 mA or 1 kilohm to protect both the DTS and the equipment under test.

EIA leads are monitored by a bridging impedance of 27 kilohms for minimal circuit loading.

A voltmeter (25-kilohm load) can be patched to any lead to read the actual voltage present (0 to 25 volts DC range).

Fixed threshold indicators of ± 3 volts can also be patched to monitor signals or other status conditions.

3-3-8. LOOP Interface. A high-level interface is provided for testing high voltage TTY current loops.

The output solid-state keyer provides both dry contact and wet (internal battery) outputs. The dry keyer will handle 300-volt loops (double 130-volt battery TTY) and up to 100 mA with inductive spike protection. The wet output connects an internal 100-volt battery and internal current regulator. Adjustment range is from 20 to 65 mA.

The $\pm$, TIP wet output position must NOT be used when other battery voltage sources are present on the Loop.

The Loop output is electrically referenced to internal circuit ground and to pin 7 of the EIA connector.

DO NOT OPERATE WITH LOOP and EIA CIRCUIT CONNECTIONS AT THE SAME TIME.

The loop input circuit is optically isolated from circuit ground. Switching thresholds are panel selected for 20 mA (10 mA Sw), 60 mA (30 mA Sw), and Polar (± 3 mA).

The meter on the analyzer will read Loop current when the input loop is connected.

Input loop impedance is approximately 100 ohms.

3-3-9. Power Supply. The internal power supply provides three regulated logic voltages, +5 volts DC, +12 volts DC, -12 volts DC, and an unregulated loop supply of 100 volts DC. There are no adjustments for power supply voltage.

230-volt operation can be obtained by operating an internal slide switch.

a. Thru Patch

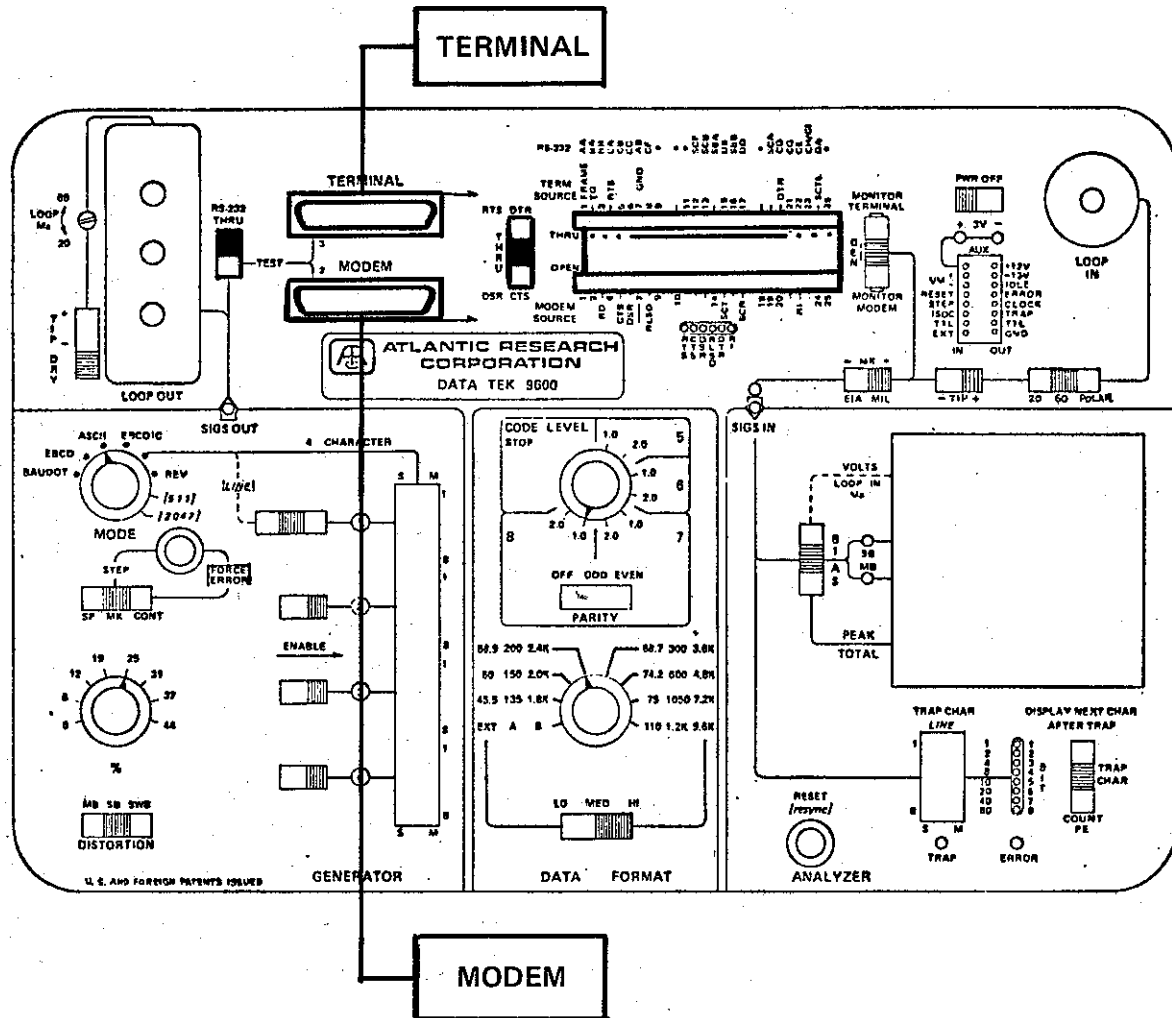


Figure 3-8a. EIA On-line Monitor.

b. Bridging Tap

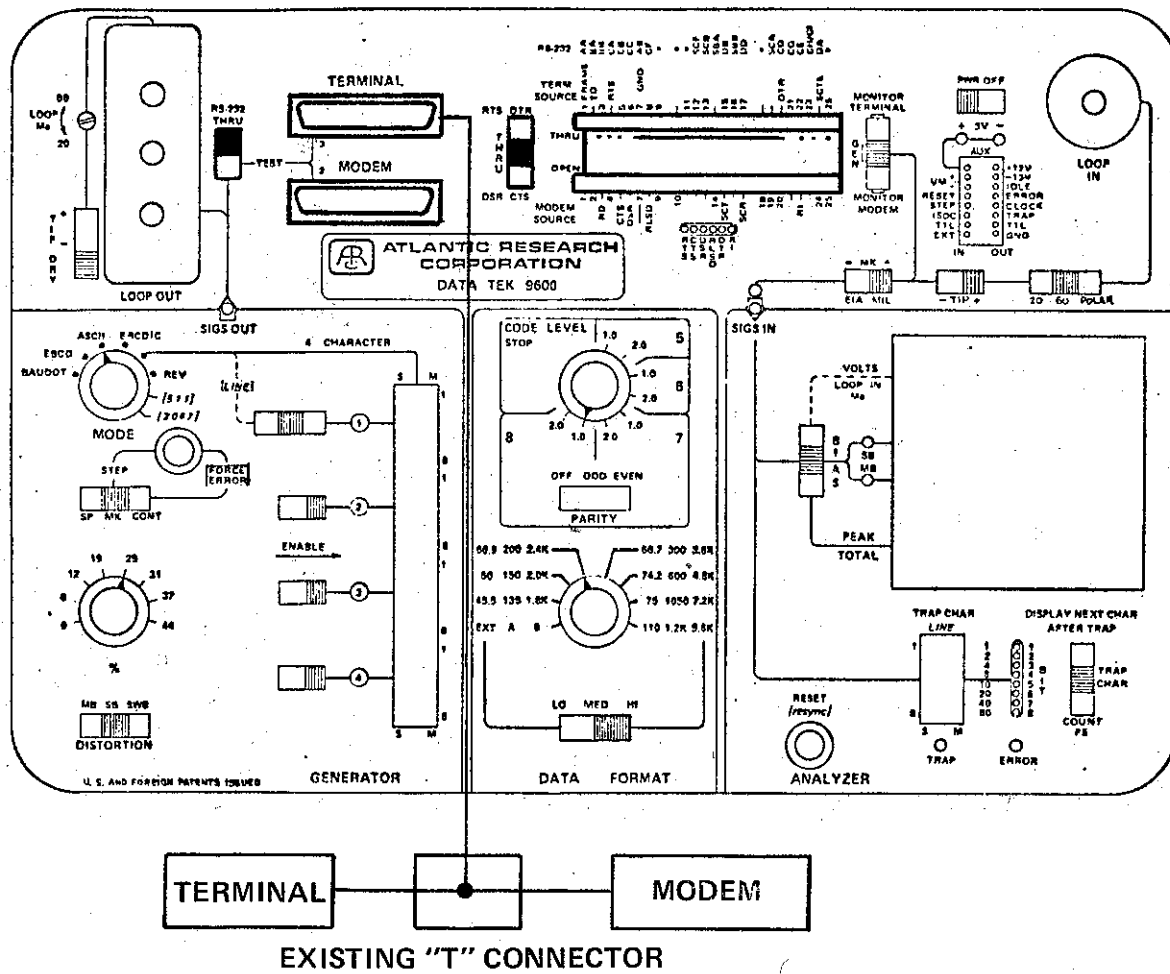


Figure 3-8b. EIA On-line Monitor

a. Terminal Test

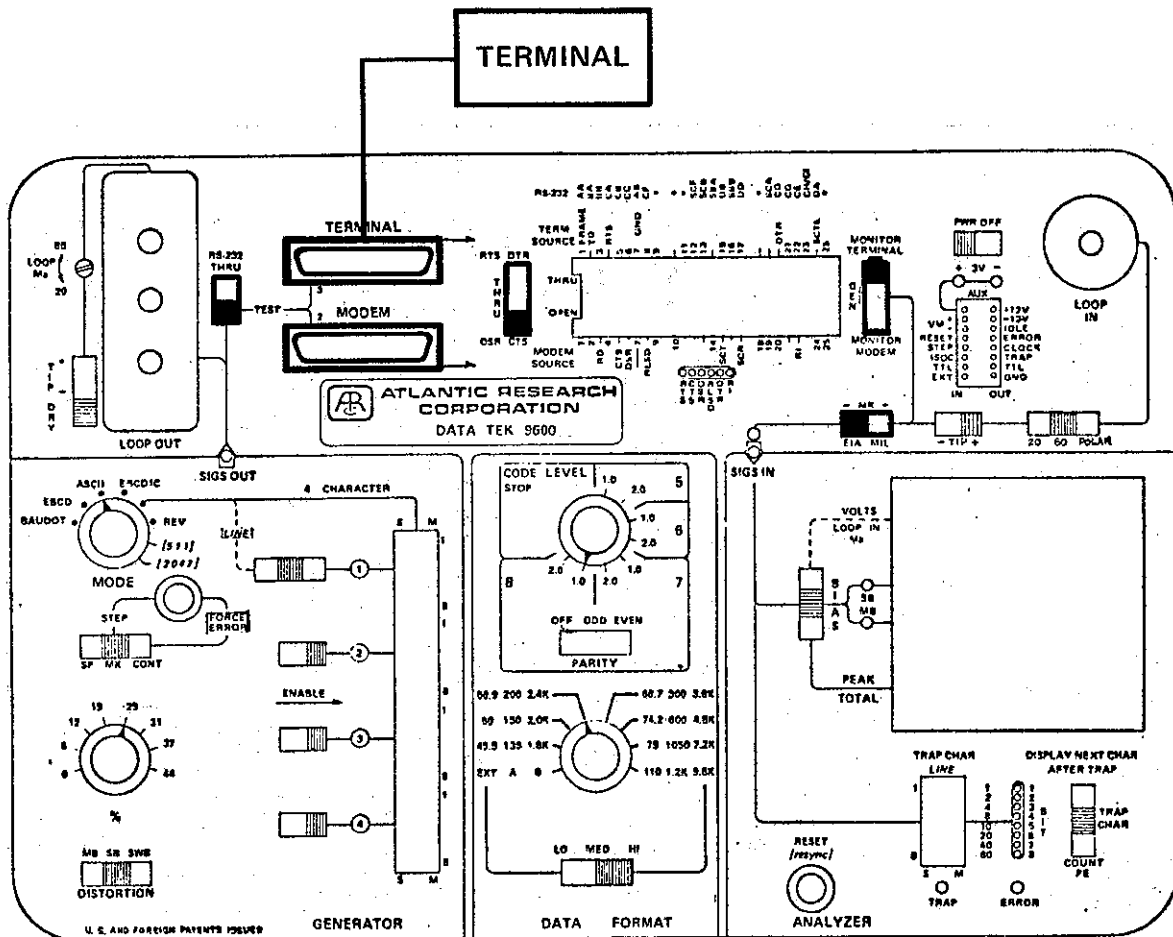


Figure 3-9a. EIA Off Line Test.

b. Modem Test

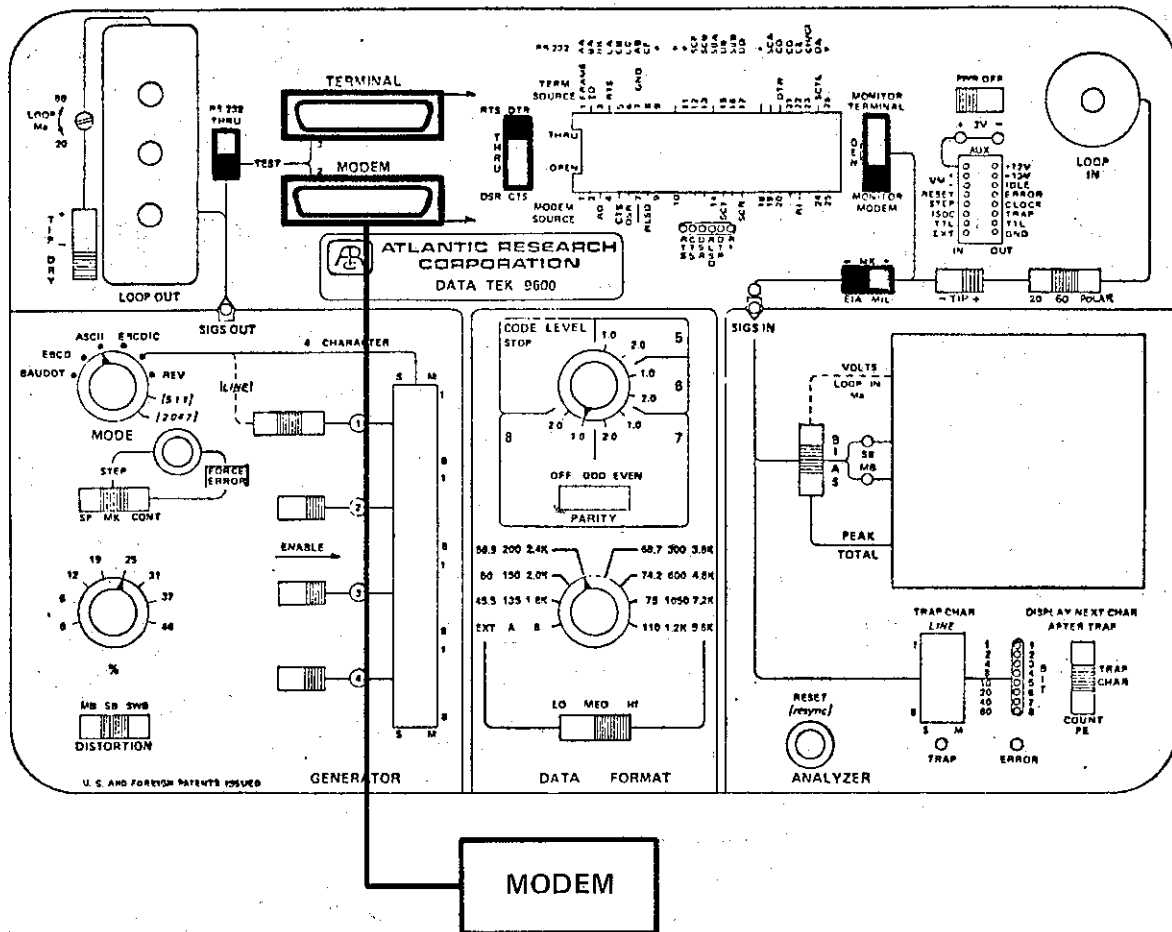


Figure 3-9b. EIA Off Line Test.

a. Monitor Jack Available

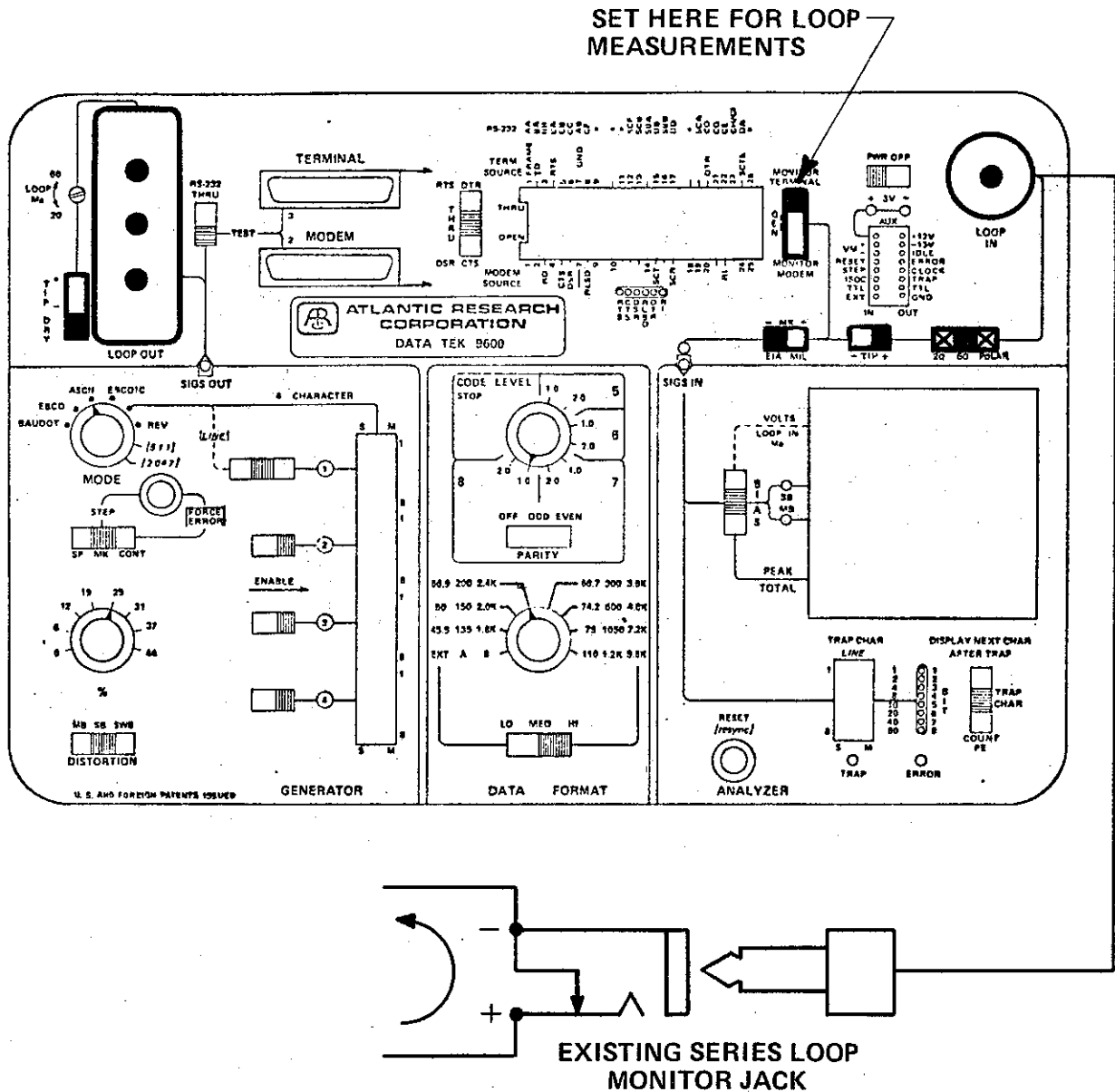


Figure 3-10a. Loop Access.

b. Monitor Jack not Available

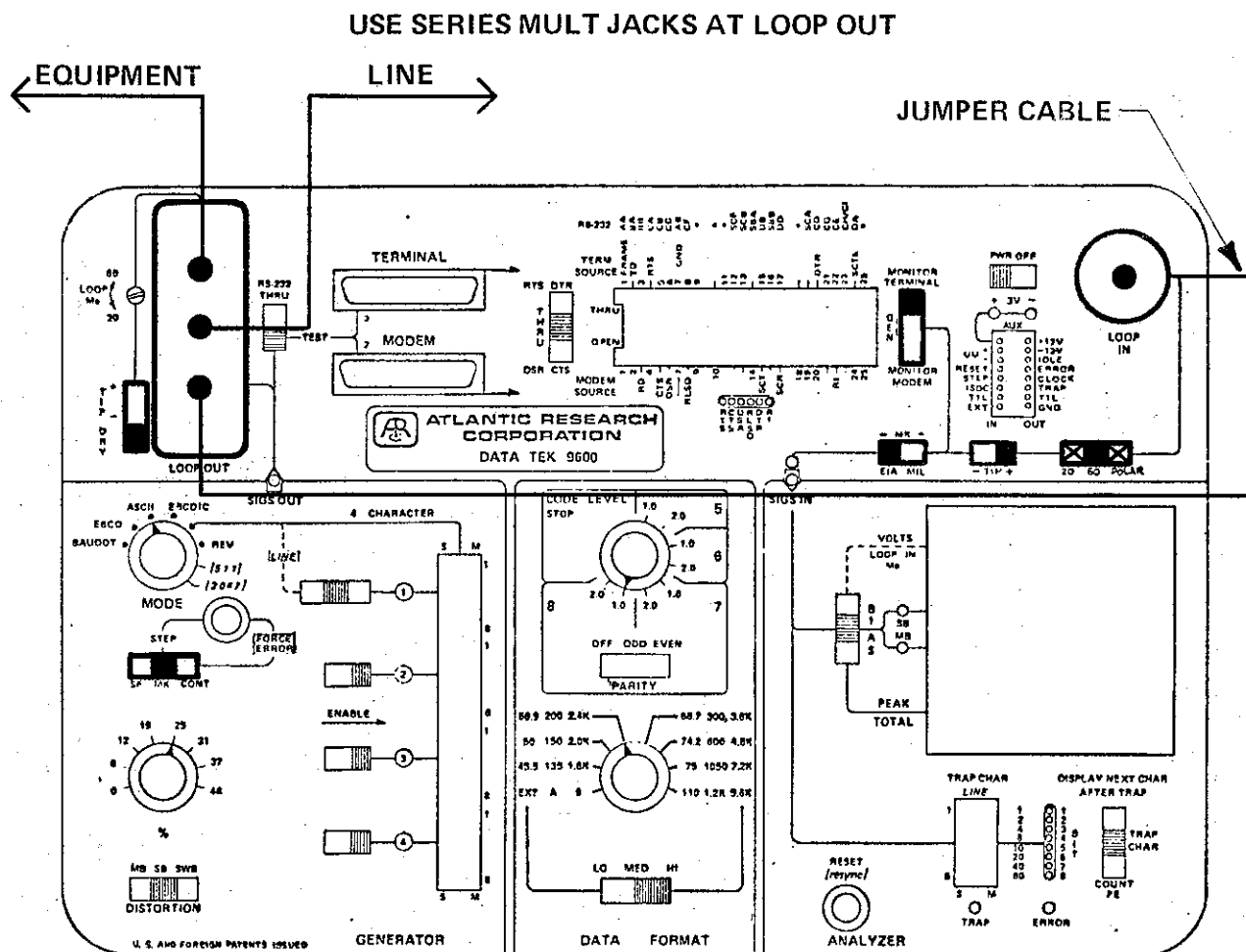


Figure 3-10b. Loop Access.

c. Off Line Measurements

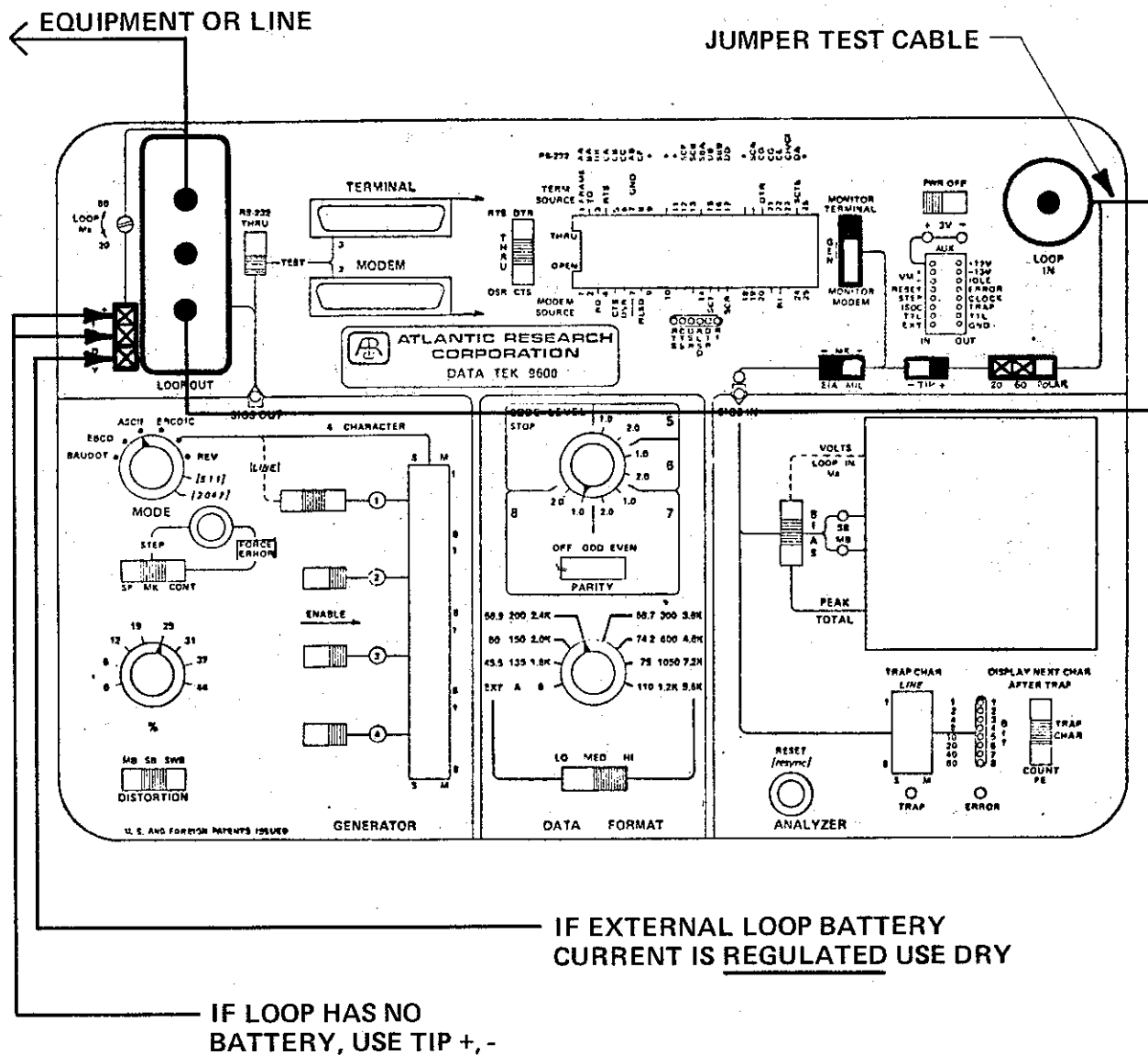


Figure 3-10c. Loop Access.

a. EIA Voltage

FOR NEGATIVE REVERSE $\pm$ VM LEADS

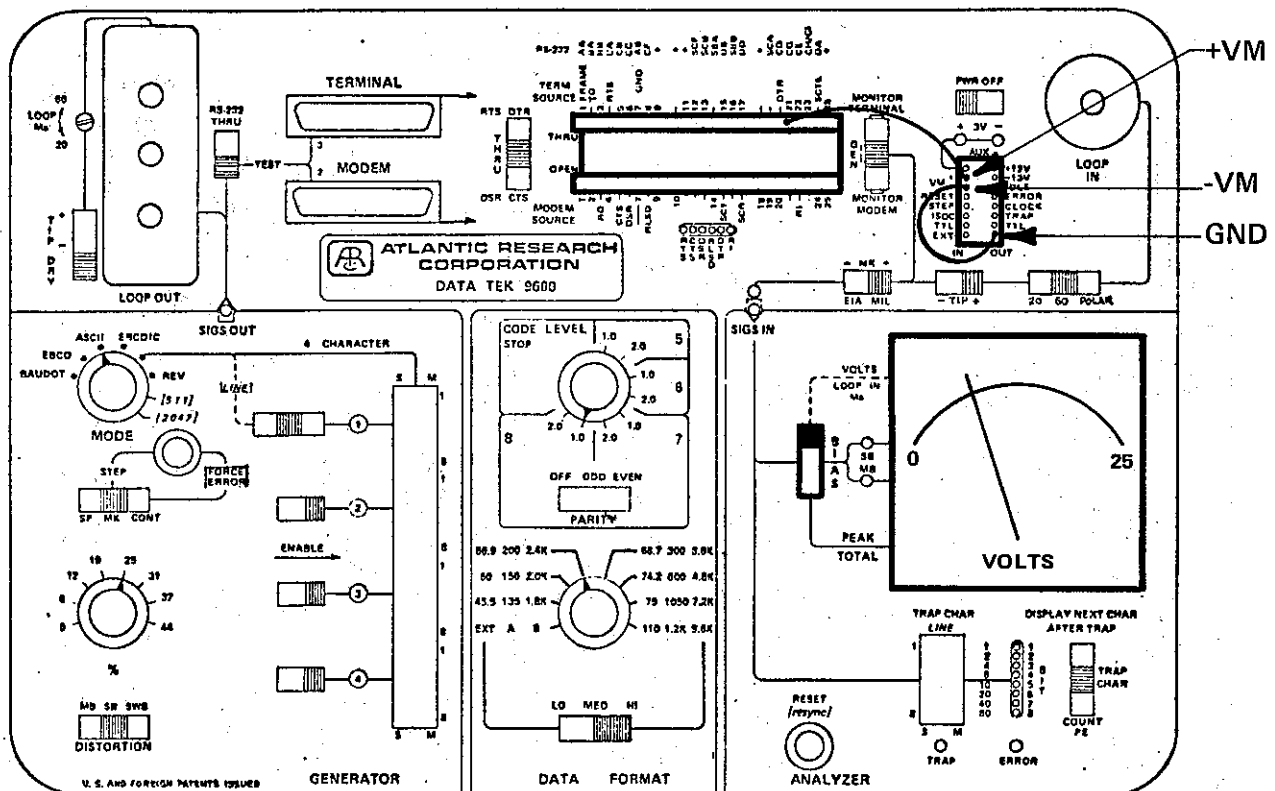


Figure 3-11a. On-line Measurements.

b. Loop Current

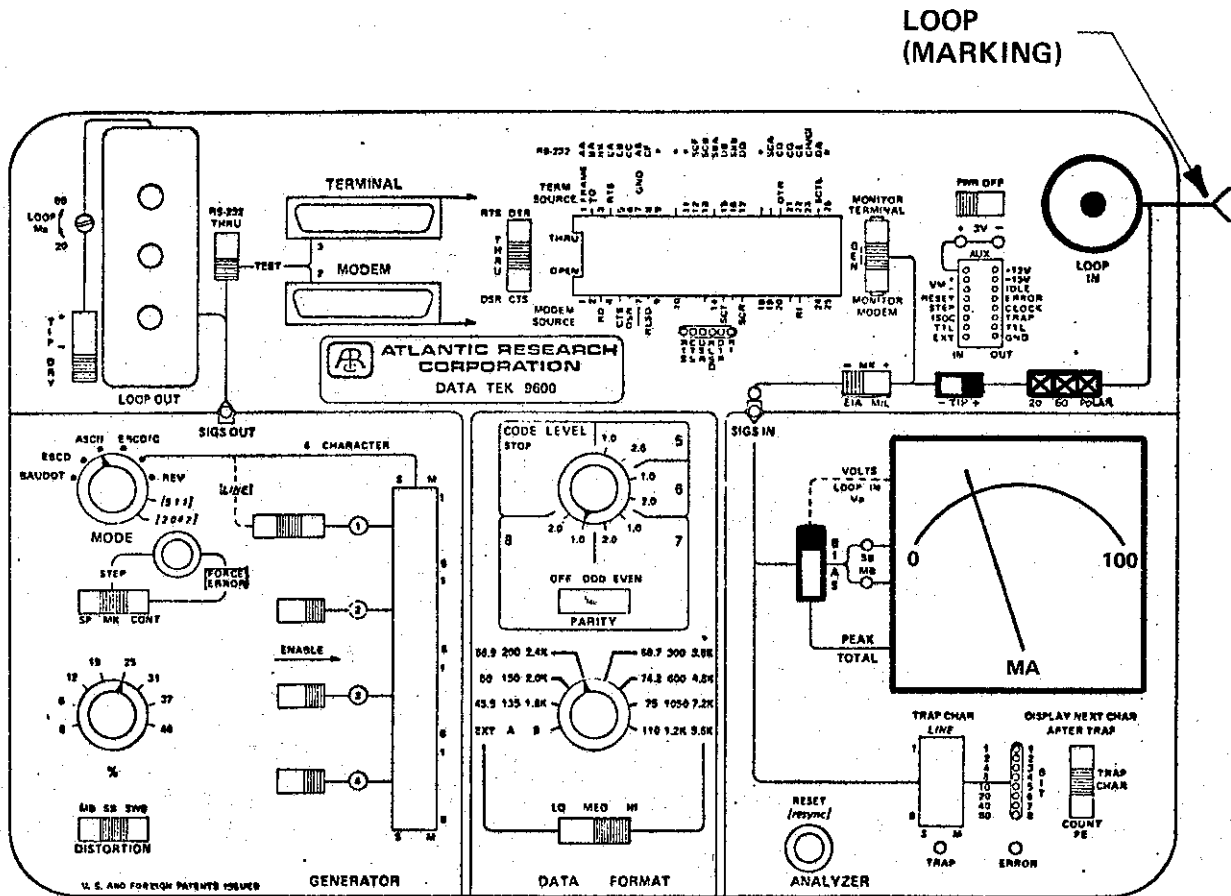
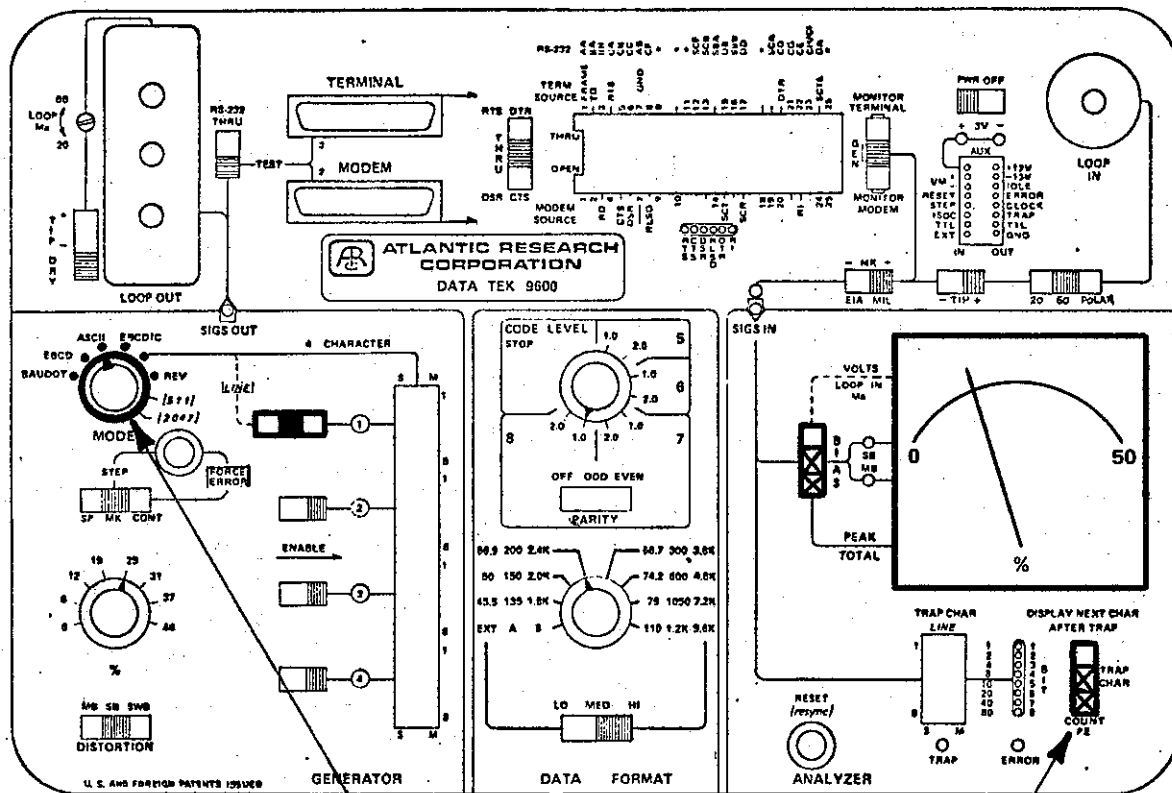


Figure 3-11b. On-line Measurements

c. Distortion



DATA
MODE

STOPS READING AFTER CHAR
AFTER TRAP CHAR

Figure 3-11c. On-line Measurements.

d. Character Trap

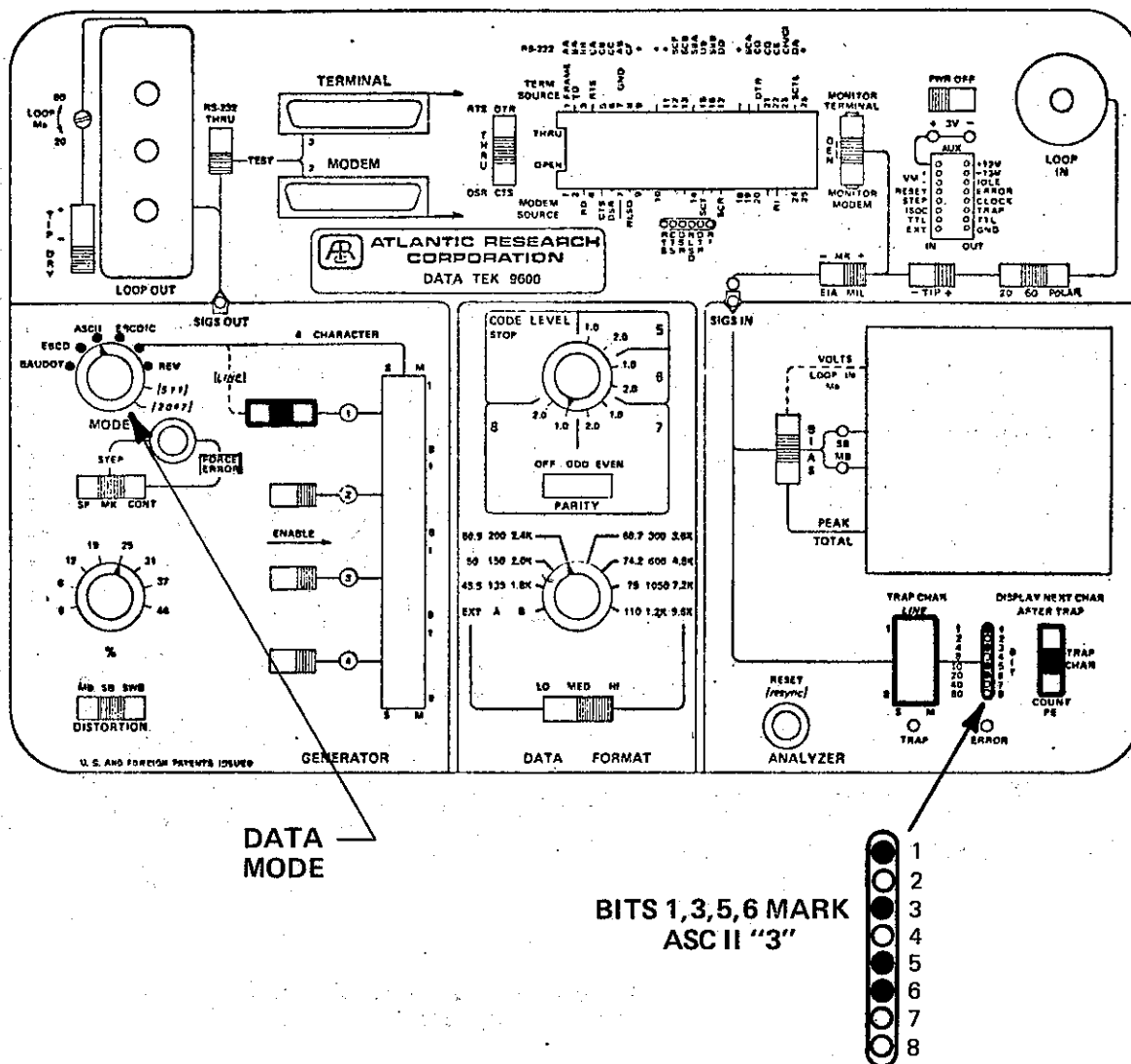


Figure 3-11d. On-line Measurements

e. CERT

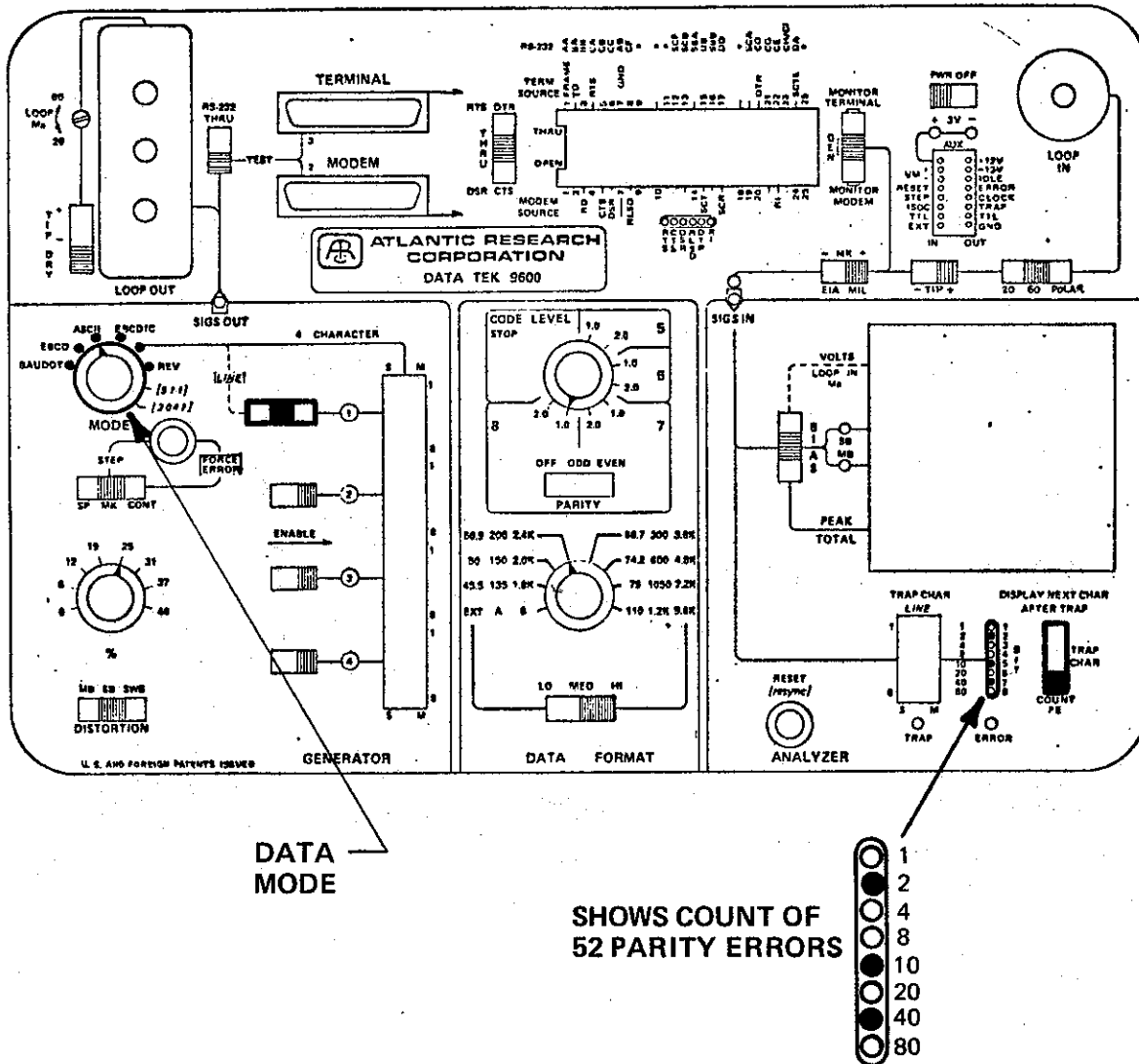


Figure 3-11e. On-line Measurements.

a. Terminal Test with Distortion Threshold

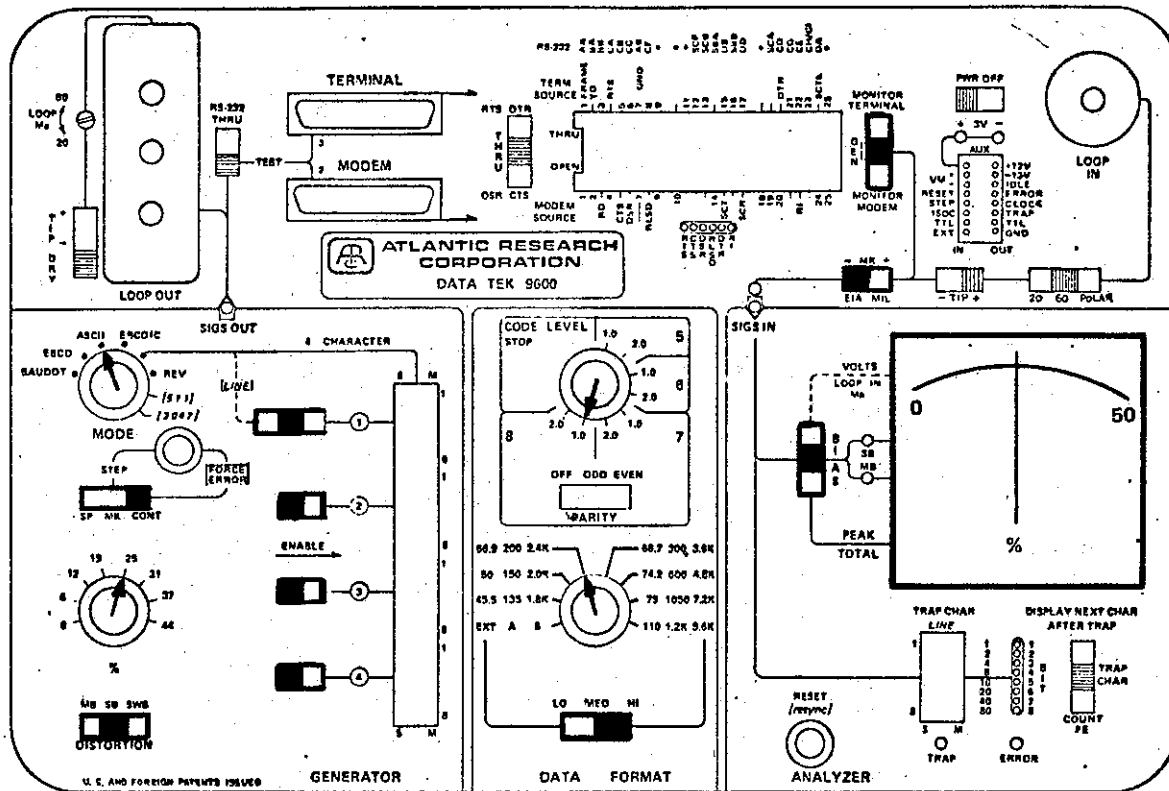


Figure 3-12a. Terminal Tests.

b. POLL Terminal: "ABCD" Sequence

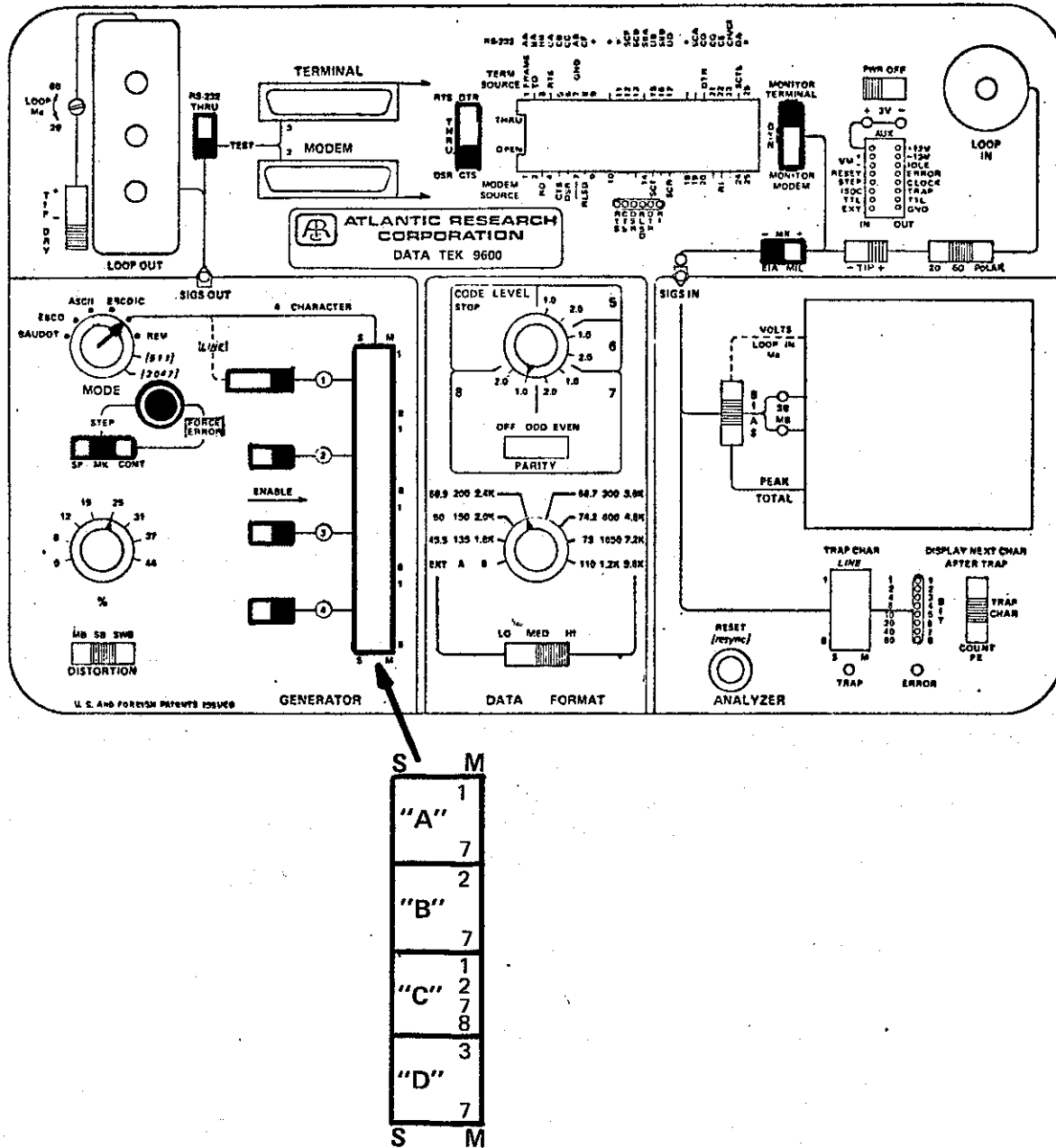


Figure 3-12b. Terminal Tests

c. Verification of Keyboard Characters

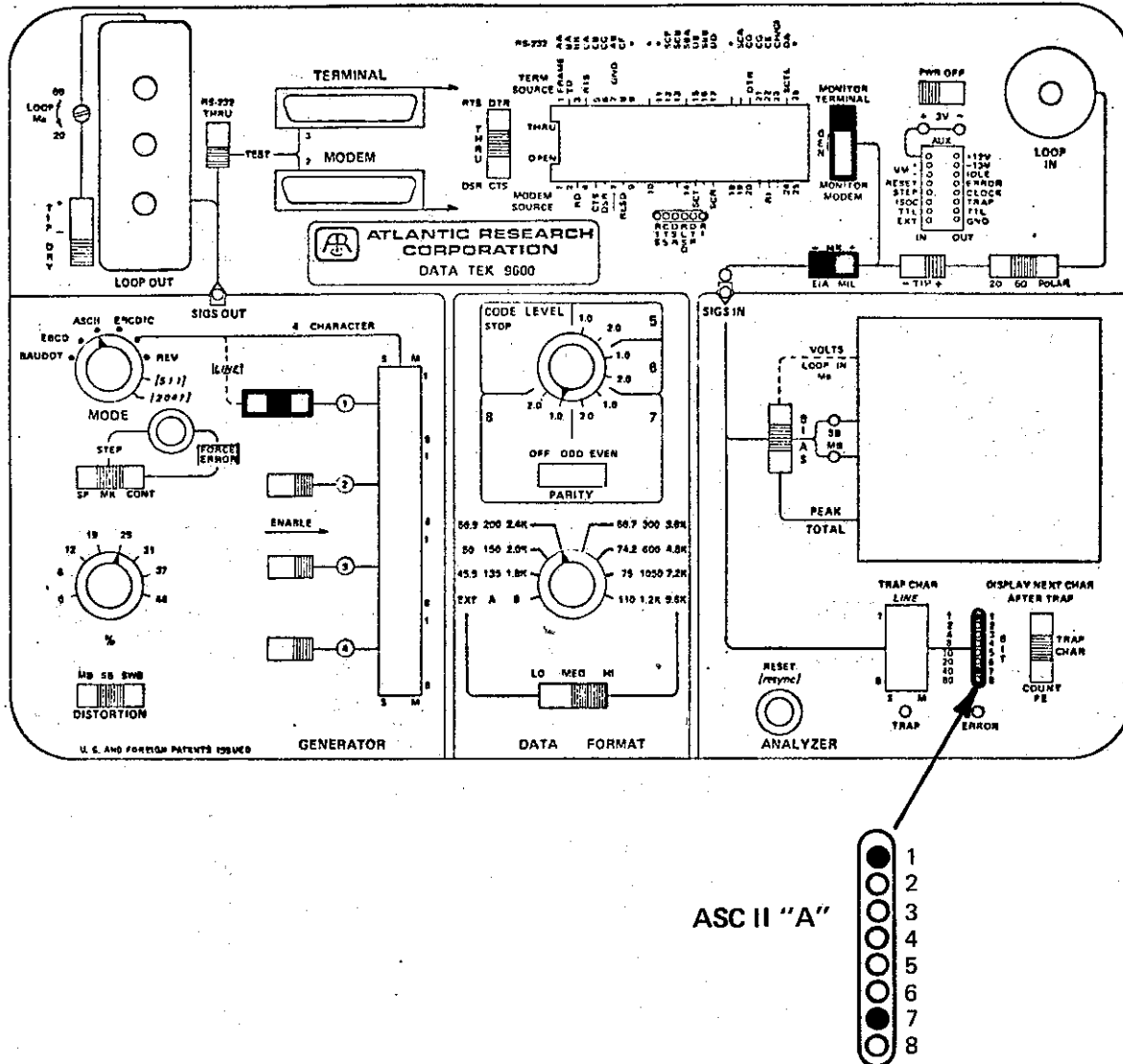


Figure 3-12c. Terminal Tests.

d. Trap Answerback Answers "AC"

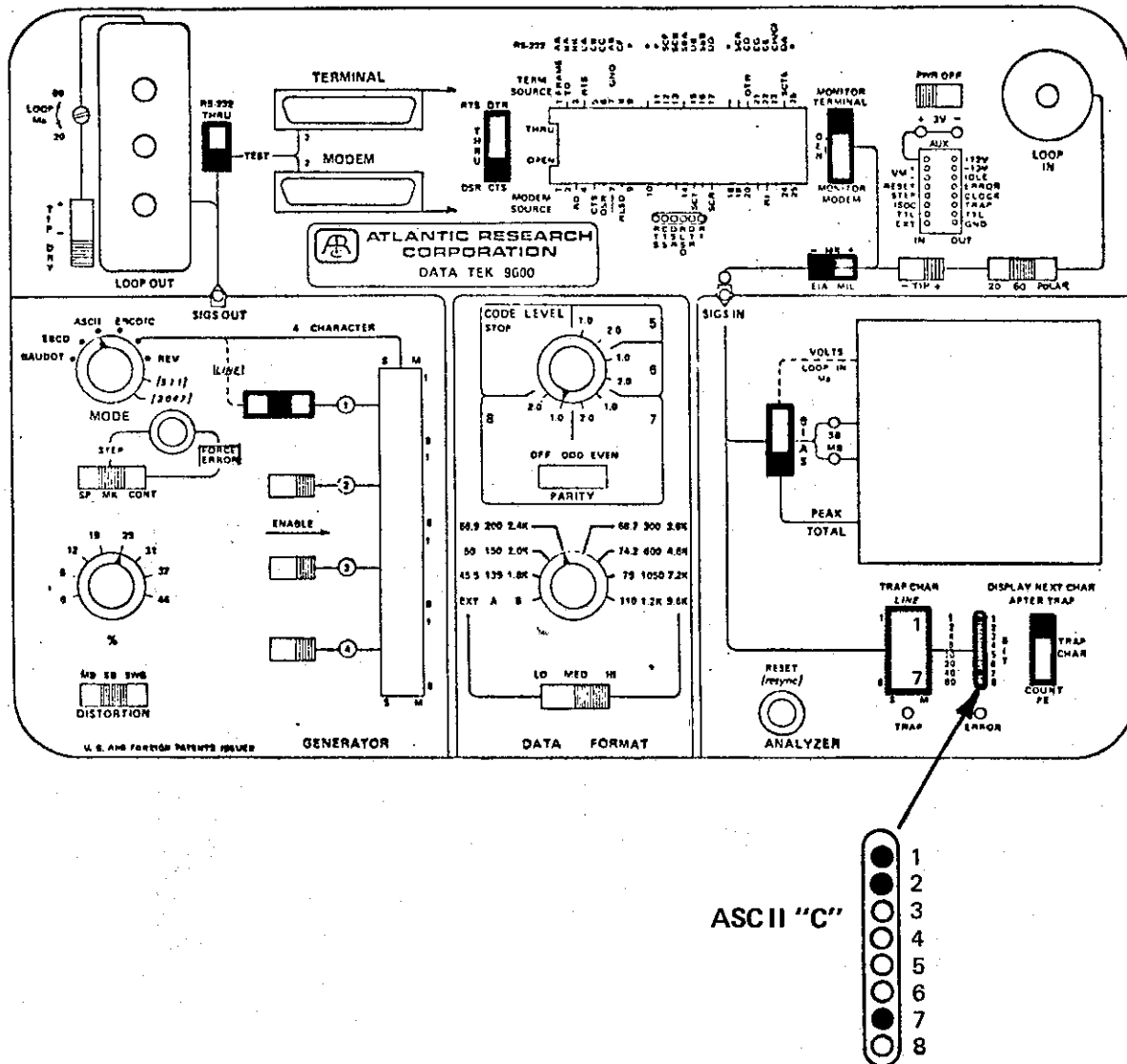


Figure 3-12d. Terminal Tests.

a. 96-Character Line

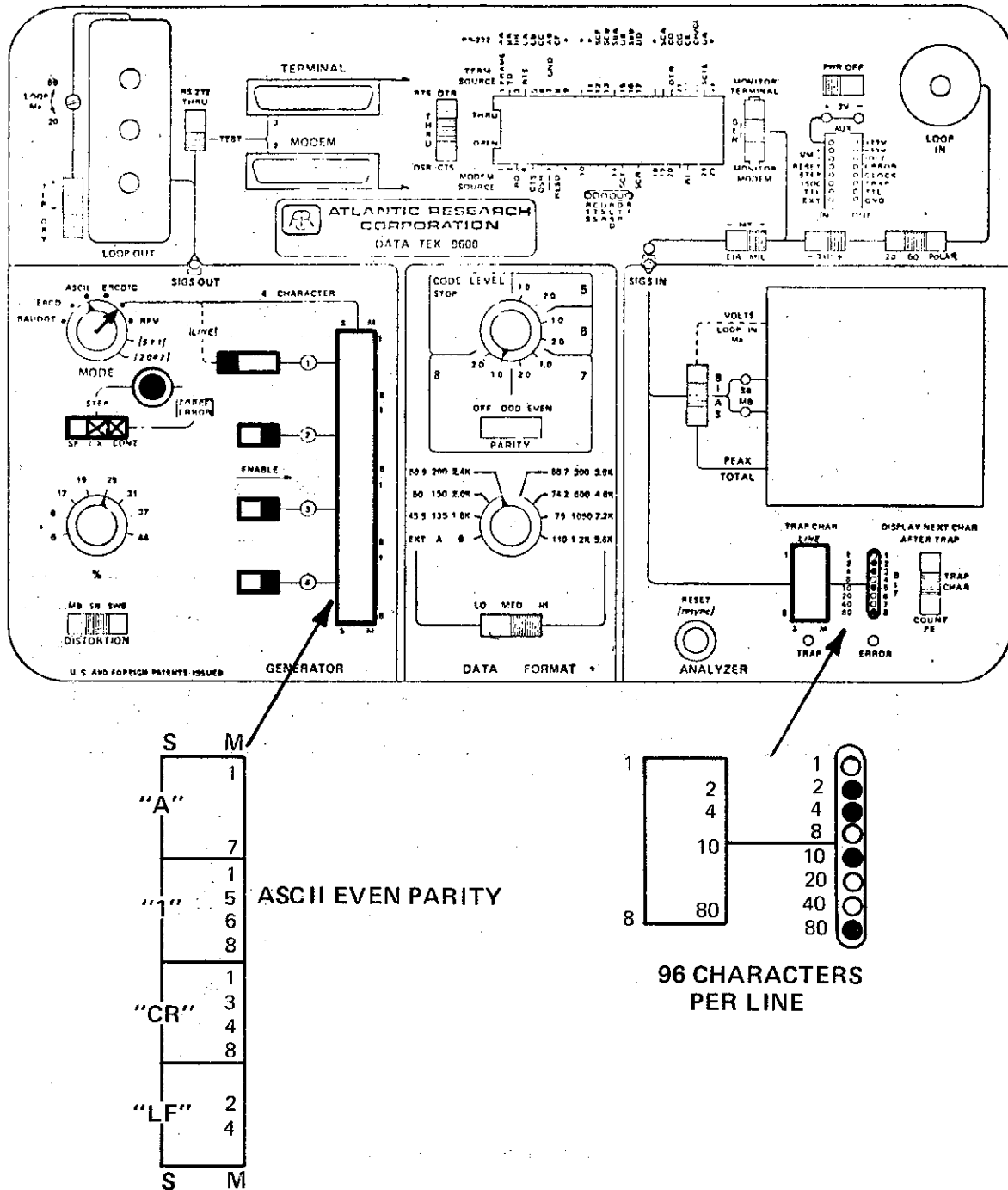


Figure 3-13a. Printer Tests.

a. Synchronous Bert

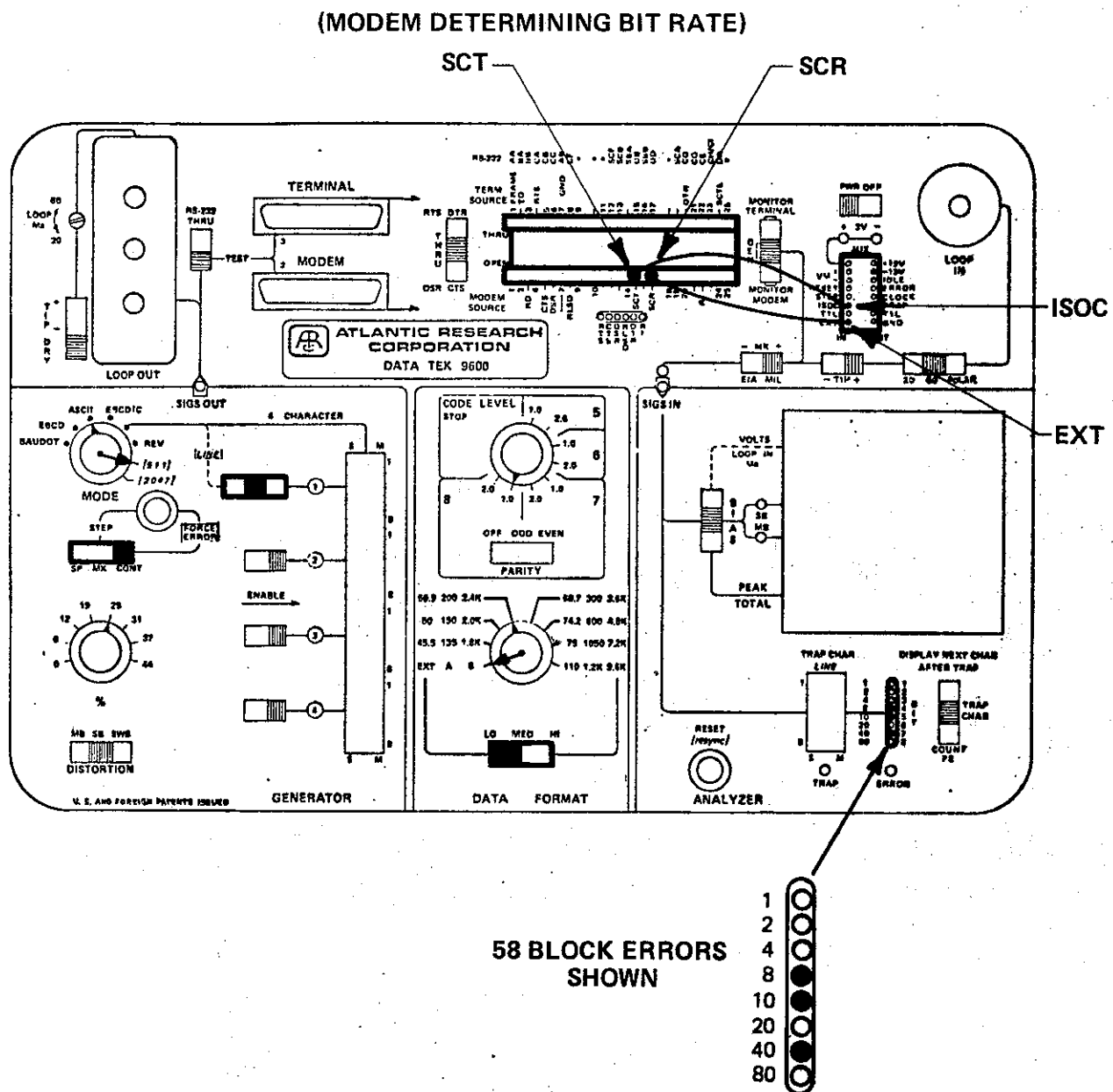
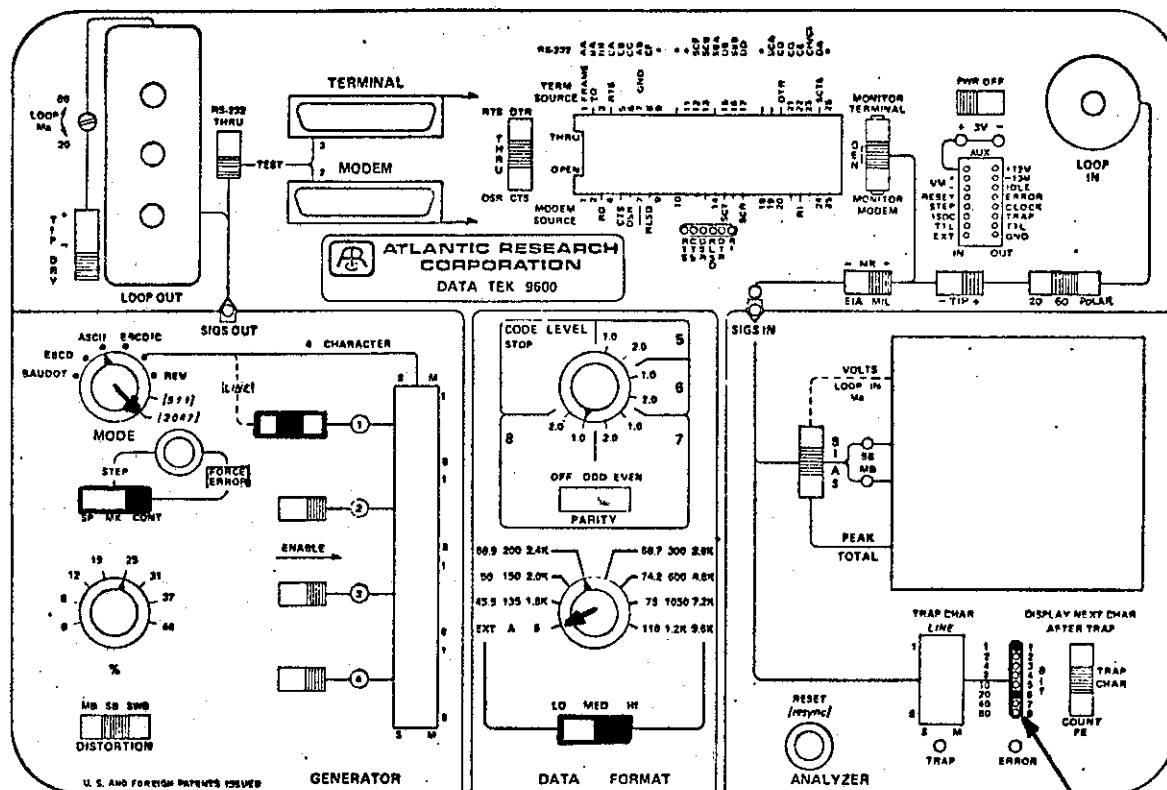


Figure 3-14a. Transmission Tests.

b. Asynchronous Bert

(1200 BAUD)



21 BLOCK ERRORS
SHOWN

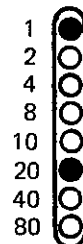


Figure 3-14b. Transmission Tests.

c. Isochronous Data Mode

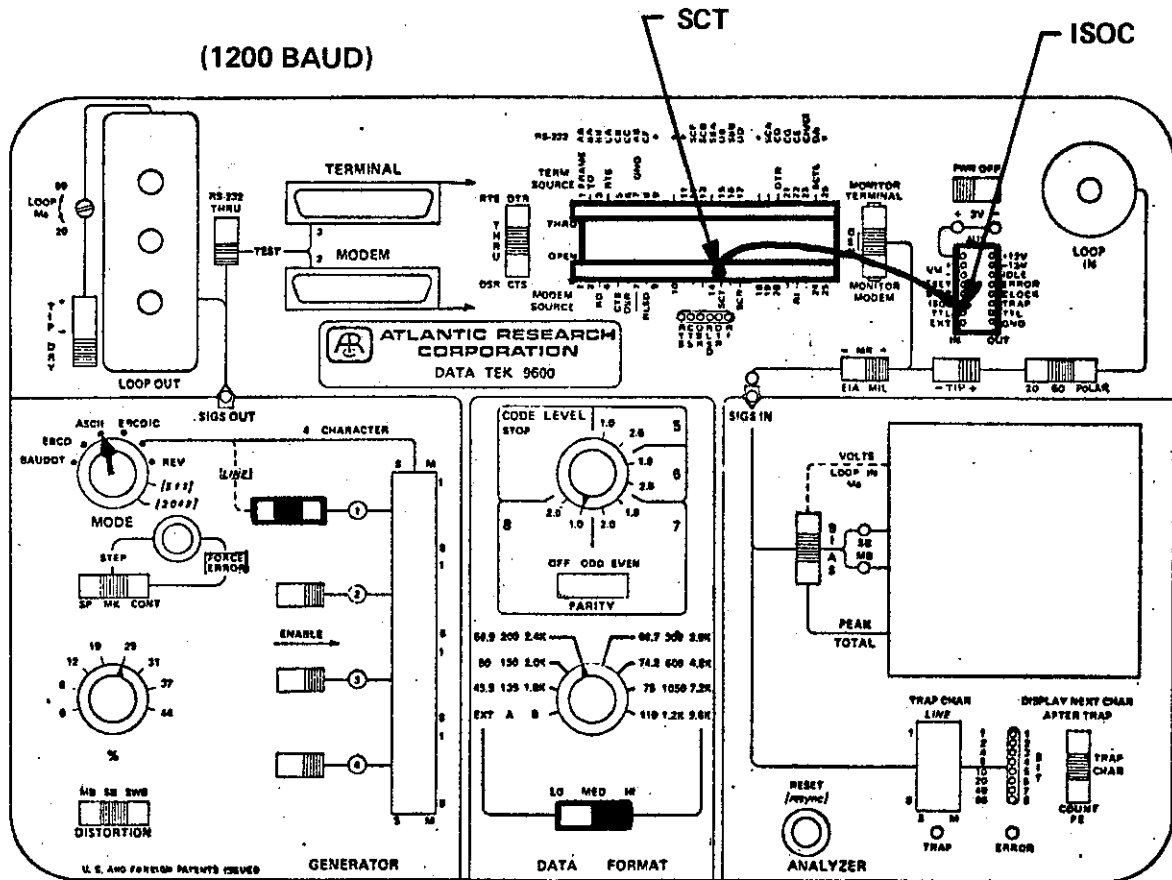


Figure 3-14c. Transmission Tests.

TM 833

SECTION IV

THEORY OF OPERATION

This section describes the operation of the basic functions of the DTS. Certain logic elements are utilized in different ways depending upon the operating mode of the DTS. Figure 4-1 shows an overall block diagram of the logic in the DTS.

Data and clock signal paths are shown as they apply to the 511-2047 and the data modes.

4-1. Data Mode. The data mode functions are shown in Figures 4-2 and 4-3.

Messages to be transmitted are contained in a ROM (Read Only Memory) chip and the 4-character switches on the front panel. These parallel signals are serialized by the data transmitter. The serial output of the data transmitter then has distortion introduced in controlled amounts as selected by the panel distortion switch.

The transmitter can send the message continuously or as a STEP, e.g., after one transmission the output will revert to idle mark. Operation of the STEP switch will release another transmission of 64 characters, 4 characters, or one line of characters as selected.

Reversals are generated by a single flip-flop without distortion.

The output signals are connected to three output drivers for interfacing to external equipment: Loop Keyer, EIA ± 12 -volt driver, TTL logic buffer.

Data signals into the analyzer are obtained from four sources: TTL logic buffer, LOOP IN isolator, EIA input amplifier, the Generator.

At the logic level, signals are presented to two circuits: the serial-to-parallel converter receiver and the distortion analyzer.

Parallel data from the receiver is displayed by bit lights and compared to the TRAP bit switches. Agreement causes the trap light to come ON.

The comparator is disconnected from the receiver data bits in the count PE position and is connected to a parity error counter. The comparison is still operable and the trap light can be used to indicate that a preset threshold is exceeded.

The distortion analyzer processes only the space-to-mark transitions in BIAS and continually updates the meter. All transistons are analyzed in PEAK/TOTAL and update the meter only if they exceed the pre-existent distortion displayed by the meter.

511-2047 Mode utilizes a separate psuedo-random generator and analyzer, as shown in Figure 4-1. The analyzer is similar to the generator except that the incoming signal is compared to the internal generator to determine the presence of errors.

Each complete block consists of 511 or 2047 bits which are repeated.

Block errors are defined as 1-bit error (or more) within the block.

Block or bit errors must be counted and displayed on the panel lights (maximum count of 159). The preset threshold can be selected for the number of tolerable errors after which the TRAP light will come on.

The analyzer is manually synchronized to the incoming data pattern. The resync switch must be operated for no longer than 1/2 second at any bit rate to achieve sync. The error light indicates each bit error.

When no clock is provided (non-synchronous data sets), the analyzer derives clock from the received signal by phase correction of the internally generated bit rate clock.

4-2. LINE MODE. The LINE MODE causes the generator and analyzer to operate in unison to achieve an output signal.

The output signal is generated by the transmitter as in the Data Mode using 4 characters.

Characters 1 and 2 are repeated until the desired line is full, e.g., 1 to 159 characters per line. Each transmitted character is counted and the count compared to the Trap LINE value. When equality is determined, the trap light comes ON to indicate a match and end of line. The trap light is then reset when characters 3 and 4 are sent (usually containing CR/LF).

The distortion analyzer and generator are operative in this mode of operation to enable testing of printers.

4-3. EIA Interface. The EIA interface is provided by using buffer amplifiers. Figure 4-4 shows the equivalent circuits of the EIA keyer and EIA receiver. The loading of the EIA signal to be monitored is approximately 27 kilohms, resistive. The EIA output keyer is a constant-current source limited to 10 to 20 mA. Output voltages are usually ± 11 volts, thereby providing adequate protection against introducing failures into other equipment via erroneous connections. Other EIA leads are forced ON via +12 volts supplied through a 1 kilohm limiting resistor.

The schematic representation of the RS-232 wiring in the DTS is shown in Figure 4-4a and b.

4-4. LOOP Interface. The LOOP interface requires the two circuits shown in Figure 4-4c and d.

DRY output signals are generated by a high voltage transistor, polarity protected by a bridge rectifier, *current* protected by a 10-ohm 1/4-watt resistor, and *inductive spike* protected by a 300-volt zener.

When + or - TIP output is selected, a 100-volt DC power supply is inserted into the output keyer loop along with a current regulator. The current regulator uses the front panel as a heat sink to eliminate internal heating.

Loop input signals are isolated by an optical coupler. The input coupler is diode-protected against current surges. A series 100-ohm resistor is contained in the loop input as a shunt to measure loop current.

4-5. Clock Conventions. Clock conventions are very important. This paragraph will treat both EIA interface clock conventions as well as the bit rate generator within the DTS.

Clock at the EIA interface conforms to the RS-232 specification, e.g., the negative transition occurs at the mid-point of the data bit. Skew at 9600 baud is only a few percent of the bit width.

Figure 4-1 shows the clock paths for the analyzer and generator. For the normal data mode, the internal bit rate generator supplies clock to the transmitter, receiver and distortion analyzer. An external clock at a frequency of 128 times the bit rate is required, e.g., at 1200 bits per second use $64 \times 1200 =$ a frequency of 76,800 Hz. This clock should be greater than 3 volts RMS but the duty cycle and waveform are of no consequence.

The AUX ISOC input is connected to the modem transmit clock to phase synchronize the transmitted data bits with SCT. This rephasing is only applicable to the bit rates shown on the front panel.

Clock for the 511-2047 mode can be derived from the internal oscillator for asynchronous modems (that don't contain a clock path). The received data signal causes the internal analyzer clock to be rephased.

When clock is provided by a synchronous modem, the SCT (pin 15) is patched to the generator via the AUX ISOC pin and SCR (pin 17) is patched to the analyzer via the AUX EXT pin. The bit rate must select EXT in the synchronous mode.

4-6. Bit Rates. Bit rates are selected by the BIT RATE switch on the front panel.

4-7. Special Speeds. DATA-TEK offers the capability for the user to specify two special speeds marked "A" and "B" on the Data Format section of the panel. These are ordered as customer options.

The accuracy of these speeds can be calculated by dividing the BIT rate into 57600. The error is equal to the remainder as a percentage of the entire number resulting from the division process."

Example: Bit rate desired is 475 baud

$$\frac{57600}{475} = 121.263$$

$$\% \text{ error} = \frac{0.263}{121.263} = 0.216\%$$

The range of the speeds selectable is from 14 baud to 9600 baud.

4-8. Power. Electronic regulation is provided for the +12-, -12-, and +5-volt supplies. The 100-volt loop supply is not voltage-regulated since a current regulator is provided as part of the LOOP interface.

Input voltage may be selected from 115 or 230 volts AC by an internal slide switch on the bottom PC board.

Brownout voltages down to 85 volts will still permit the DTS to operate properly.

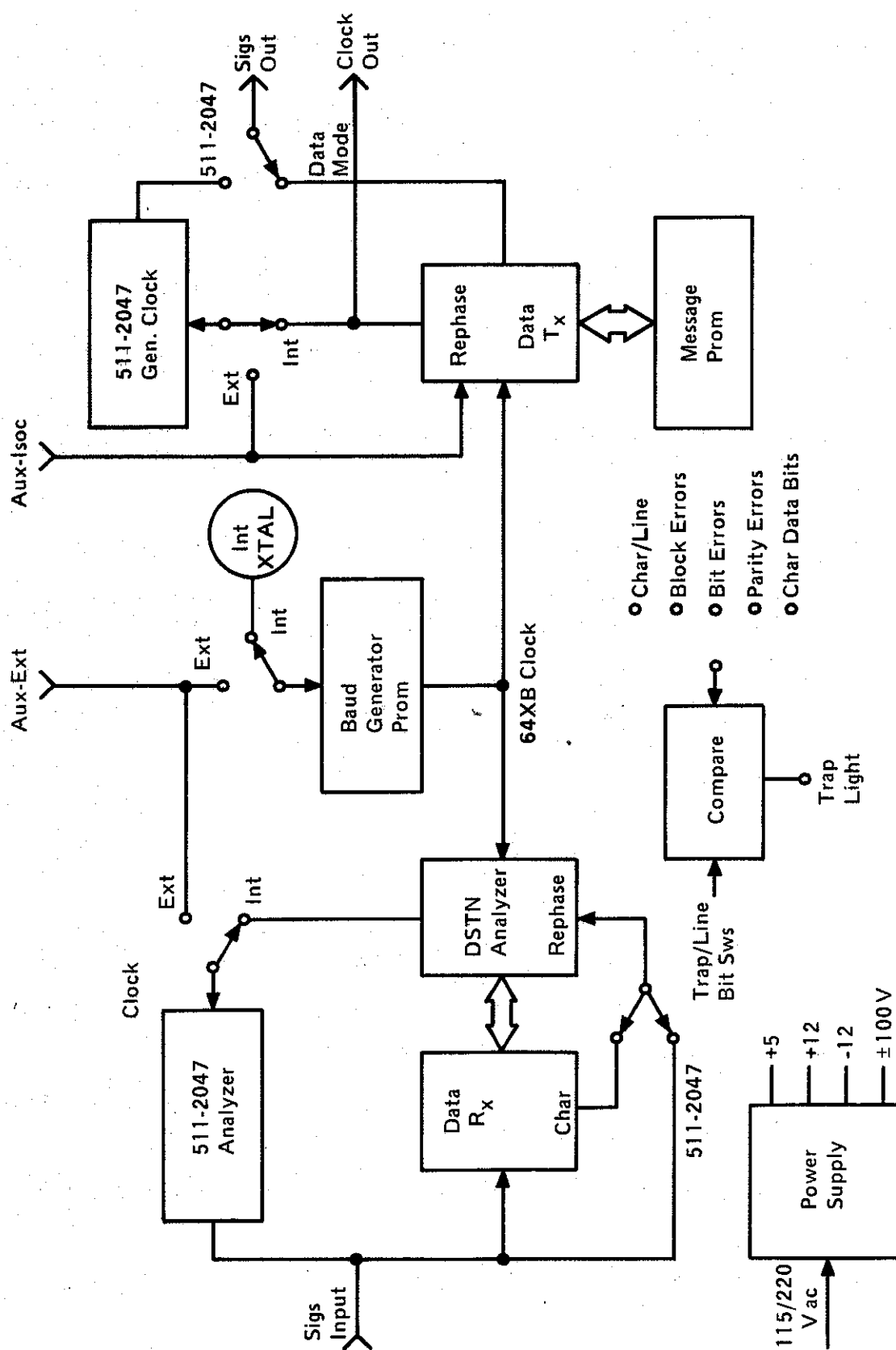


Figure 4-1. Data TEK 9600 Block Diagram.

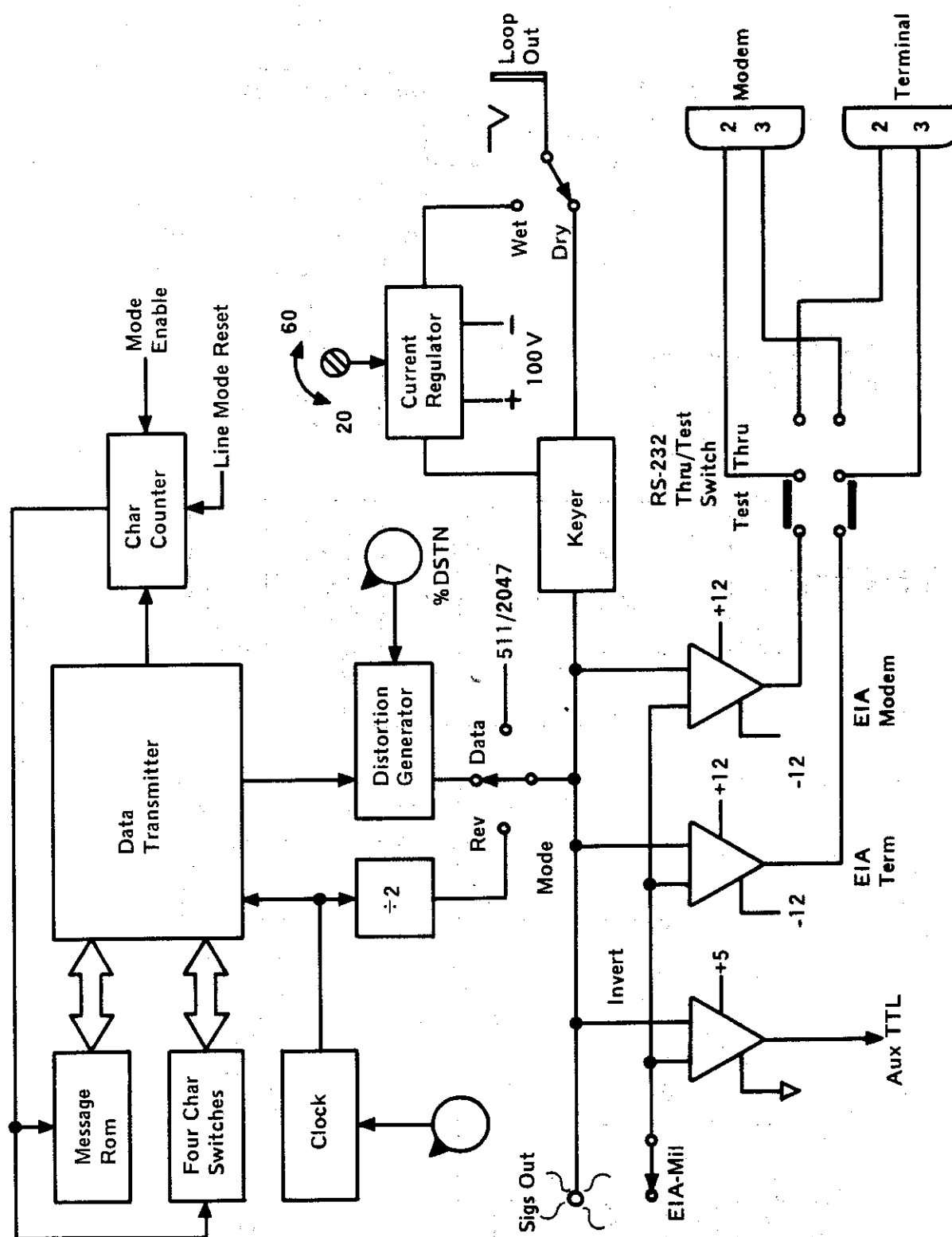


Figure 4-2. Data Mode Generator.

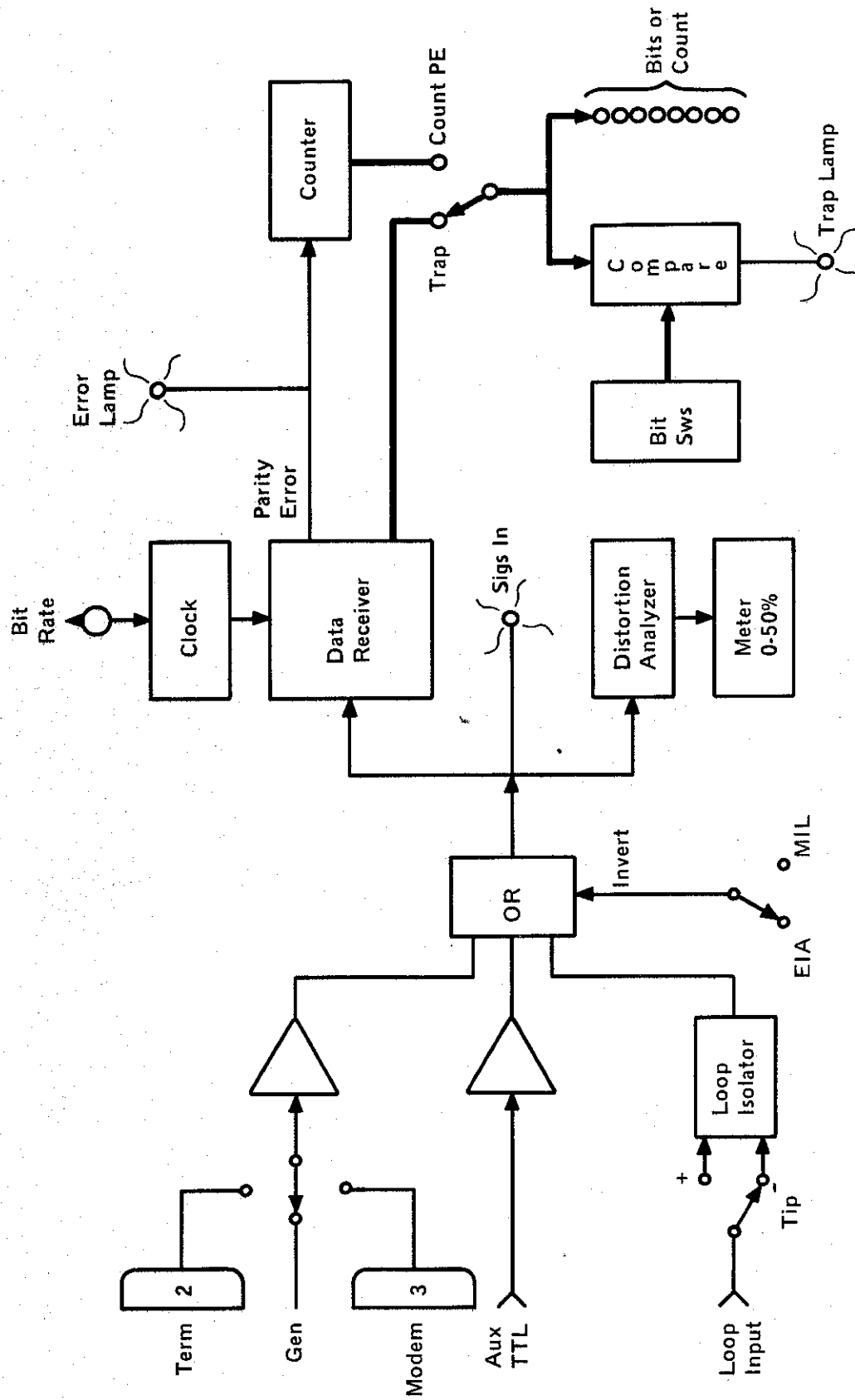


Figure 4-3. Data Mode Analyzer.

4-9. Output Specification and Input Requirements

4-9-1. Data Signal Interface. Data signals may be applied to the DTS in three types: EIA, LOOP, TTL logic levels. Table 1-1 lists these characteristics.

4-9-2. Auxiliary Interface. Other electrical signals can be used to control or monitor the DTS operation through the auxiliary interface. These characteristics are shown in Table 1-2.

4-9-3. Electrical Interface. The electrical interface is shown schematically in Figure 4-4 for the RS-232 and Loop signals. Figures 4-5 and 4-6 show the auxiliary interface for INputs and OUTputs, respectively.

4-10. Stored Messages. The contents of the four 64-character "FOX" stored messages are shown below.

DATA-TEK 9600 (DTS-1-1, 2,3: PROM 833C-001)

BAUDOT

(LTR) (LTR) (LTR) (LTR) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) OVER (SP)
A (SP) LAZY (SP) DOG (SP) (SP) (FIGS) 1234567890 (SP) (LTR) DE (CR) (LF)

BAUDOT HEXADECIMAL

FF	FF	FF	FF	F0	F4	E1	E4	F7	E7	E6	EE	EF	E4	F9	EA
F8	F3	EC	E4	ED	F8	FD	E4	EB	E7	FC	F6	E5	E4	F8	FE
E1	EA	E4	E3	E4	F2	E3	F4	F5	E4	E9	F8	FA	E4	E4	FB
F7	F3	E1	EA	F0	F5	E7	E6	F8	F6	E4	FF	E9	E1	E8	E2

EBCD (SEVEN LEVEL)

(DEL) (DEL) (DEL) (DEL) (UC) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) OVER
(SP) A (SP) LAZY (SP) DOG (SP) (SP) (LC) 1234567890 (SP) (UC) DE (NL)

EBCD HEXADECIMAL

FF	FF	FF	FF	DC	F2	C7	EB	C0	C5	CA	E7	F3	D1	C0	D3
E5	D9	DA	E9	C0	DB	D9	FA	C0	E1	CA	C9	F9	D2	C0	D9
EA	EB	E5	C0	E3	C0	F1	E3	E6	C6	C0	CB	D9	FB	C0	C0
DF	E0	D0	F0	C8	E8	D8	F8	C4	E4	D4	C0	DC	CB	EB	ED

ASCII

(R0) (R0) (R0) (R0) The (SP) Quick (SP) Brown (SP) Fox (SP) Jumps (SP) Over (SP) A (SP) Lazy
(SP) Dog (SP) (SP) 1234567890 (SP) TEST (CR) (LF)

ASCII HEXADECIMAL

FF	FF	FF	FF	D4	E8	E5	A0	D1	F5	E9	E3	EB	A0	C2	F2
EF	F7	EE	A0	C6	EF	F8	A0	CA	F5	ED	F0	F3	A0	CF	F6
E5	F2	A0	C1	A0	CC	E1	FA	F9	A0	C4	EF	E7	A0	A0	B1
B2	B3	B4	B5	B6	B7	B8	B9	B0	A0	D4	C5	D3	D4	8D	8A

EBCDIC (EIGHT LEVEL)

(NU) (NU) (NU) (NU) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) OVER (SP) A
 (SP) LAZY (SP) DOG (SP) (SP) 1234567890 (SP) (SP) TEST (NL)

EBCDIC HEXADECIMAL

FF	FF	FF	FF	E3	88	85	40	D8	A4	89	83	92	40	C2	99
96	A6	95	40	C6	96	A7	40	D1	A4	94	97	A2	40	D6	A5
85	99	40	C1	40	D3	81	A9	A8	40	C4	96	87	40	40	F1
F2	F3	F4	F5	F6	F7	F8	F9	F0	40	40	E3	C5	E2	E3	15

DATA-TEK 2400 (DTS-1-4: PROM 833C-002)

BAUDOT

(LTR) (LTR) (LTR) (LTR) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) OVER (SP)
 A (SP) LAZY (SP) DOG (SP) (FIGS) 1234567890 (SP) (LTRS) DE (CR) (LF) (LTRS)

BAUDOT HEXADECIMAL

FF	FF	FF	FF	F0	F4	E1	E4	F7	E7	E6	EE	EF	E4	F9	EA
F8	F3	EC	E4	ED	F8	FD	E4	EB	E7	FC	F6	E5	E4	F8	FE
E1	EA	E4	E3	E4	F2	E3	F1	F5	E4	E9	F8	FA	E4	FB	F7
F3	E1	EA	F0	F5	E7	E6	F8	F6	E4	FF	E9	E1	E8	E2	FF

EBCD (SEVEN LEVEL)

(DEL) (DEL) (DEL) (DEL) (UC) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) OVER
 (SP) A (SP) LAZY (SP) DOG (SP) (LC) 1234567890 (SP) (UC) DE (SP) (NL)

EBCD (HEXADECIMAL)

FF	FF	FF	FF	DC	F2	C7	EB	C0	C5	CA	E7	F3	D1	C0	D3
E5	D9	DA	E9	C0	DB	D9	FA	C0	E1	CA	C9	F9	D2	C0	D9
EA	EB	E5	C0	E3	C0	F1	E3	E6	C6	C0	CB	D9	FB	C0	DF
E0	D0	F0	C8	E8	D8	F8	C4	E4	D4	C0	DC	CB	EB	C0	ED

ASCII

(R0) (R0) (R0) (R0) The (SP) Quick (SP) Brown (SP) Fox (SP) Jumps (SP) Over (SP) A (SP) Lazy
(SP) Dog (SP) 1234567890 (SP) (SP) TEST (CR) (LF)

ASCII HEXADECIMAL

FF	FF	FF	FF	D4	E8	E5	A0	D1	F5	E9	E3	EB	A0	C2	F2
EF	E7	EE	A0	C6	EF	F8	A0	CA	F5	ED	F0	F3	A0	CF	F6
E5	F2	A0	C1	A0	CC	E1	FA	F9	A0	C4	EF	E7	A0	B1	B2
B3	B4	B5	B6	B7	B8	B9	B0	A0	A0	D4	C5	D3	D4	8D	8A

TTS (SIX LEVEL)

(Shift) THE (SP) QUICK (SP) BROWN (SP) FOX (SP) JUMPS (SP) (Unshift) over (SP) a (SP) lazy
(SP) dog (SP) 1234567890 (SP) (Shift) DE (Return) (Elevate)

TTS HEXADECIMAL

FF	FF	FF	FF	DB	D0	D4	C1	C4	D7	C7	C6	CE	CF	C4	D9
CA	D8	D3	CC	C4	CD	D8	DD	C4	CB	C7	DC	D6	C5	C4	DF
D8	DE	C1	CA	C4	C3	C4	D2	C3	D1	D5	C4	C9	D8	DA	C4
FD	F3	E1	EA	F0	F5	E7	E6	F8	F6	C4	DB	C9	C1	C8	C2

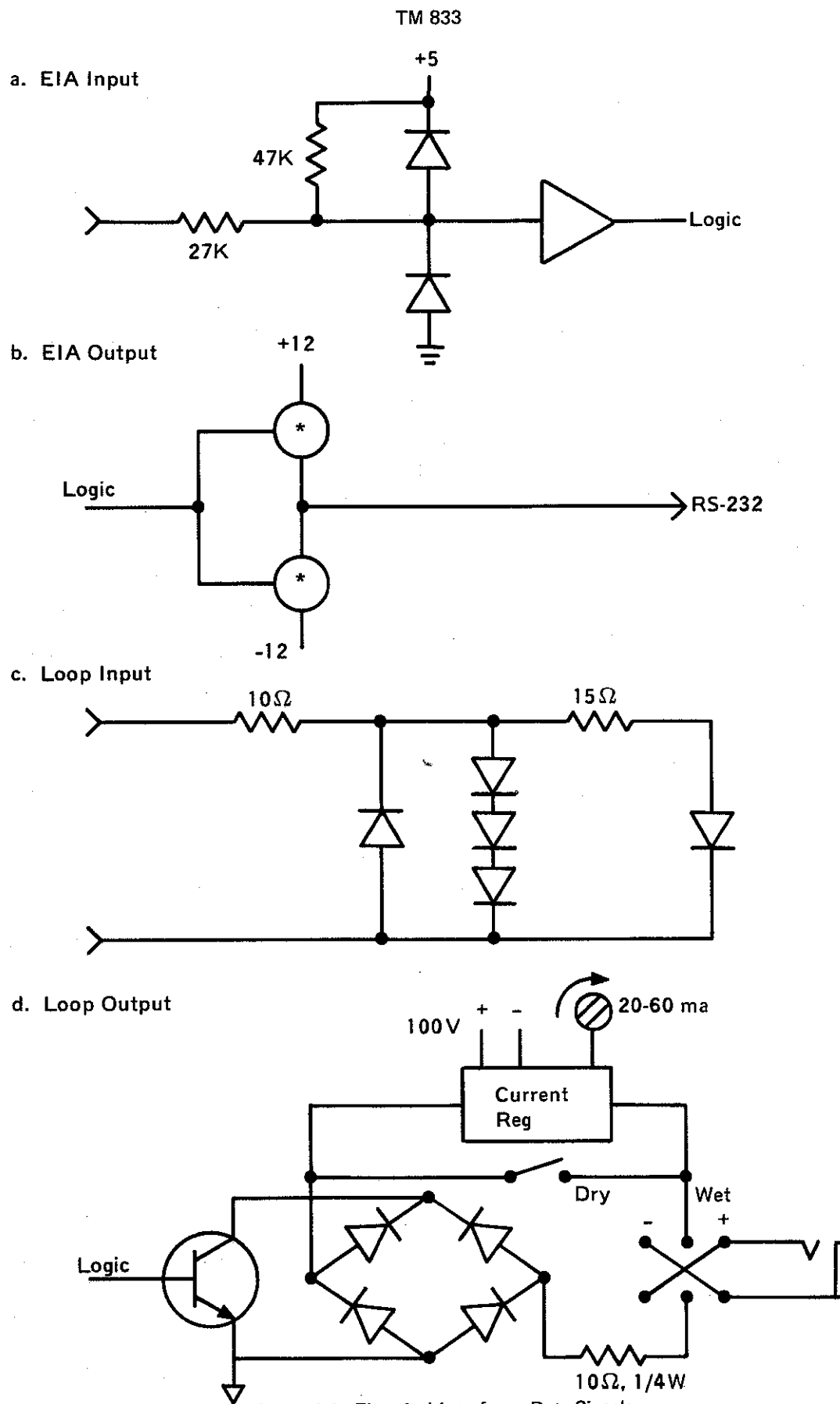
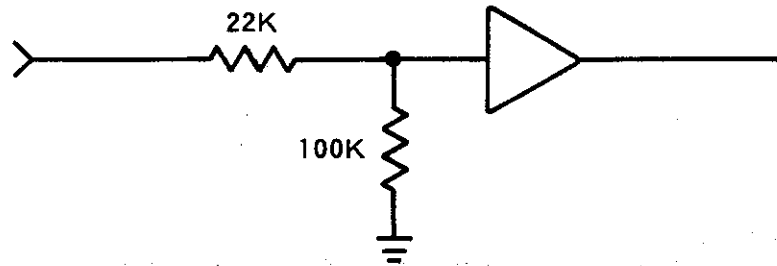
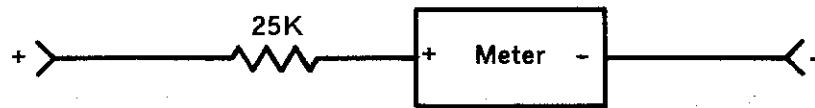


Figure 4-4. Electrical Interface: Data Signals.

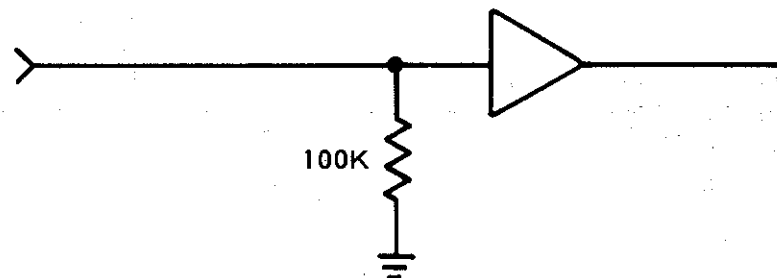
a. $\pm 3V$



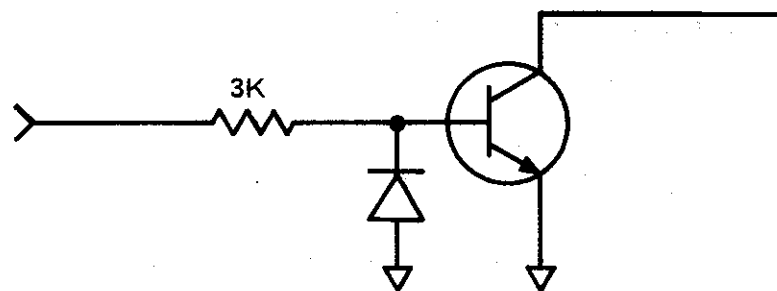
b. $\pm V_m$



c. Reset Step



d. Isoc Ext



e. TTL

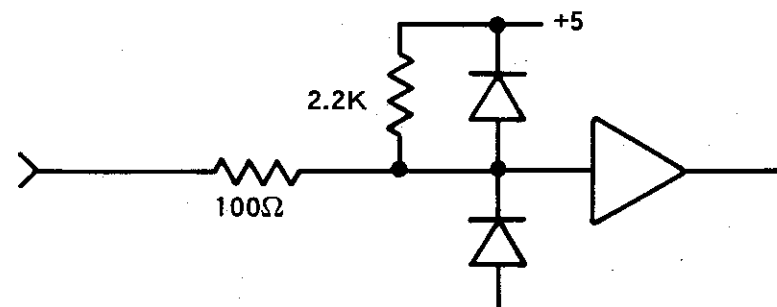


Figure 4-5. Electrical Interface - Inputs.

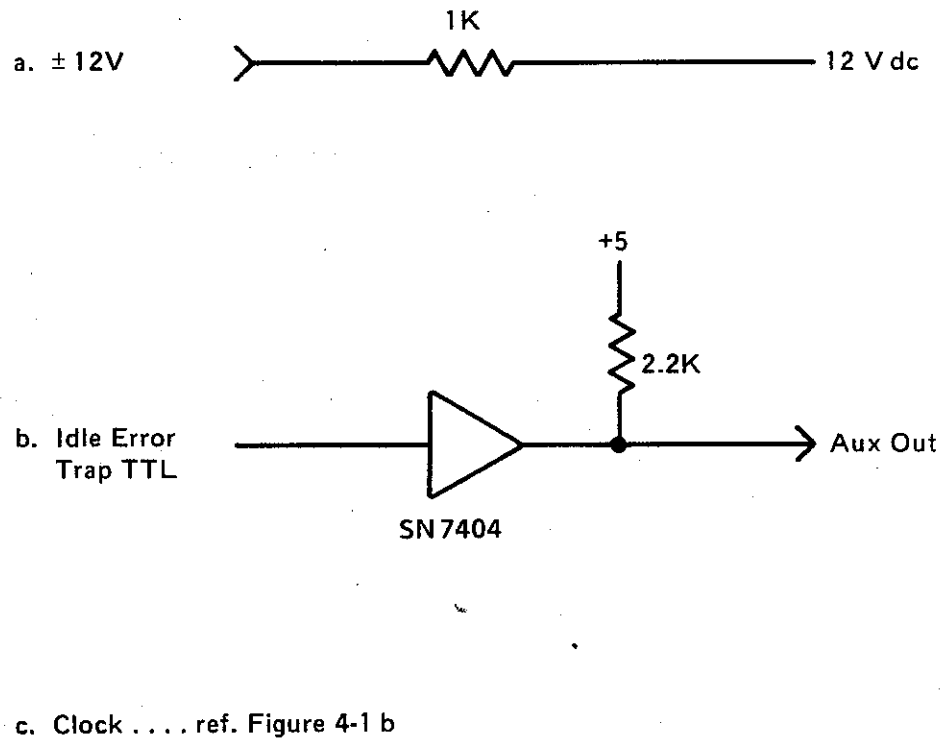


Figure 4-6. Electrical Interface - Outputs.

SECTION V

MAINTENANCE

5-1. General. This section describes the self-test features of the DTS. Repair of the DTS in the field should be limited to replacement of fuses, DIP switches, and potentiometer calibration adjustments. Virtually all characteristics of the DTS may be verified using the DTS itself.

5-2. Internal Self-Tests. The DTS generator and analyzer are independent functions, thereby permitting the analyzer and generator to be interconnected for verification of each parameter of interest.

Lid instructions contain abbreviated self-test procedures to give quick assurance to the operator in the field that the unit is operating properly. These procedures are amplified further in this section.

5-3. Basic Tests. Basic tests may be performed using the AUX connector features to verify all power supply voltages, signal, and clock drivers, and the master crystal oscillator.

<u>Step</u>	<u>Action</u>	<u>Verification</u>
1	Turn POWER ON	MB or SB Analyzer light ON
2	Set Analyzer to VOLTS	
3	Set Generator to MK	
4	Set Generator MODE to ASCII	
5	Jumper AUX-Vm to AUX GND	
6	Jumper AUX+Vm to AUX +12V	Meter reads 11 volts
7	Remove Jumper from AUX +12V	
8	Jumper AUX+Vm to AUX IDLE	Meter reads 4.5 volts
9	Remove Jumpers from AUX+Vm and AUX-Vm	
10	Jumper AUX-Vm to AUX-12V	
11	Jumper AUX+Vm to AUX GND	Meter reads 11 volts
12	Set Generator MODE to REV	
13	Set Generator to CONT	
14	Set SIGS OUT RS-232 to TEST	

<u>Step</u>	<u>Action</u>	<u>Verification</u>
15	Set BIT RATE to 1200 HI	
16	JUMPER AUX $\pm 3V$ to TERMINAL SOURCE PIN #3 for SIGS	$\pm 3V$ lights ON
17	Jumper AUX $\pm 3V$ to AUX CLOCK	$\pm 3V$ lights ON

5-4. DATA Mode. The DATA Mode functions may be verified for Distortion, Parity Count, and Data Characters verified as to their Bit pattern.

<u>Step</u>	<u>Action</u>	<u>Verification</u>
1	Set Generator Switches to ASCII MODE, CONTInuous, 25% MB, Characters 1-4 and ENABLE all MARK bits	
2	Set DATA FORMAT Switches to 8-level, 2.0 Stop, Even Parity, BIT RATE 1200 HI	SIGS OUT light ON
3	Set Analyzer to PEAK/TOTAL, Display Next Character After Trap, Trap bits 1,5,6 Mark (for ASCII "1")	
4	Set Interface SIGS IN Path Switches to GEN and EIA	SIGS IN light ON
5	Operate RESET	1 8-BIT lights will follow sigs until 2 TRAP light comes ON 3 8-BIT lights 2,5,6 ON (ASCII "2" follows "1" in the standard QUICK BROWN FOX message) 4 Meter holds 25% reading
6	Set Generator to 12% SB	5 MB light is ON while RESET is depressed and latches OFF when released.
7	Set Analyzer to BIAS, TRAP CHAR	
8	Operate RESET	1 Meter drops from 25% to 12% 2 SB light is ON 3 Trap light comes ON 4 Bit lights continue to follow data
9	Set Generator to REV	
10	Set Data Format to ODD Parity, Bit rate 300, LO	
11	Set Analyzer to Count PE and Trap Bit 1+10+20 preset count threshold of 31 counts	Observe analyzer bit lights now counting 30 per second

<u>Step</u>	<u>Action</u>	<u>Verification</u>
12	Operate RESET	Count clears and restarts from 0, Trap light OFF
13	Wait approximately 1 sec to reach preset threshold of 31 errors selected by TRAP bit switches 1+10+20	Trap light goes ON after 31 counts

5-5. LINE Mode. The LINE mode gives visual indication at the end of each line.

<u>Step</u>	<u>Action</u>	<u>Verification</u>
1	Set Generator to 4 CHAR, Char 1 to LINE, CONTInuous	
2	Set Data Format to Bit Rate 300 LO, 8-level, 2.0 stop, Parity OFF	
3	Set Analyzer TRAP-LINE bit switches to the number of characters per line 1+10+20 Mark = 31	
4	Set Interface SIGS IN path to GEN, EIA	TRAP light will pulse on once a second for each 31-character line.
5	Set Analyzer LINE switches to 10+80 Mark = 90	Trap light will pulse on once for each 90-character line (3 second intervals)
6	Set Interface Sigs Out Path to RS-232 TEST	Connect printer to TERMINAL connector and observe lines printed

5-6. BERT MODE. The 511-2047 (BERT) MODE contains a separate Generator and Analyzer which can be used together to verify operation of each.

<u>Step</u>	<u>Action</u>	<u>Verification</u>
1	Set Generator to [511] MODE, CONT	
2	Set Data Format to BIT RATE 2400, HI	
3	Set Analyzer TRAP switches for an Error count threshold of 10	
4	Set Interface Sigs In path to GEN, EIA	Analyzer bit lights will be counting, ERROR light blinking
5	Operate Analyzer [RESYNC]	Analyzer bit lights OFF, Trap light OFF

<u>Step</u>	<u>Action</u>	<u>Verification</u>
6	Hold Generator FORCE ERROR Switch down	Error count will continue at the rate of 3/sec. After 3 seconds the Trap count threshold light will come ON
7	Release Force Error	Error count stops (somewhat higher than count of 10). Trap light is still ON

5-7. LOOP Current. LOOP Current Regulator adjustment is achieved by using the Analyzer LOOP mA meter.

<u>Step</u>	<u>Action</u>	<u>Verification</u>
1	Set Generator to ASCII Mode, MK	
2	Set Interface Sigs Out path to Tip + and SIGS IN path to Tip + Set Analyzer to Loop In mA	
4	Insert tip-sleeve type patch cord from LOOP IN jack to LOOP OUT	Read mA meter
5	Using small screwdriver, adjust 20 60 pot (thru panel) for correct reading on the meter	Read mA meter
6	NOTE: Range of adjustment will exceed the range of 20 to 60 mA. The selected current will be regulated automatically regardless of external or added loop resistance up to a 90-volt external drop when regulation ceases and current diminishes.	

Calibration of all adjustments may be performed in the field using only the DTS in its self-test configuration.

Removal from the Case

<u>Step</u>	<u>Action</u>
1	Remove AC power cord from outlet.
2	Remove 4 screws around outside of case.
3	The DTS can now be lifted out of the case as a single assembly. The power transformer remains mounted within the case and its cable to the DTS assembly is sufficiently long to place the DTS assembly in front of the case, Front Panel facing up.

<u>Step</u>	<u>Action</u>
4	Note that AC voltage is exposed in the area of the Power Cord connection to the PC card and in the area of the Power Switch on the Panel PC card.

5-8. Distortion. Distortion Calibration is a single Pot on the bottom PC board. The circuit is automatically correct at zero %. The adjustment is for mid-scale calibration only, thus eliminating any interactive adjustments.

<u>Step</u>	<u>Action</u>
1	Reconnect AC power cord.
2	Locate the Distortion Pot on the Front edge of the Bottom PC board. PC board.
3	Set up for Distortion by selecting: ● Generator to ASCII Mode, continuous, 25% SWB. ● Analyzer to BIAS, TRAP. ● Data Format 1200 HI, 8-level, 2.0 stop, Even Parity ● Interface sigs in Path to Gen, EIA.
4	Adjust the pot for 25% meter reading.

5-9. Switching Threshold. Input LOOP current switching threshold is adjustable for 20 mA and 60 mA.

<u>Step</u>	<u>Action</u>
1	Set up the unit as Paragraph 5-7 for loop adjustment. Set loop for 10 mA. Set Interface Sigs IN Path to monitor terminal, + Tip, EIA, 20 mA.
2	Stand the DTS assembly so the Panel is Vertical. Locate two adjustments on the top of the Panel PC board (in the vicinity) of the LOOP-IN jack.
3	Adjust the 20 mA Pot while observing the SIGS IN light. The correct setting is the threshold where the SIGS IN light just goes ON.
4	Adjust the Loop Current to 30 mA.
5	Set the Sigs IN Path to 60 mA and adjust the 60 mA Pot while observing the SIGS IN light. The correct setting is the threshold where the SIGS IN light just goes ON.

5-10. External Test Equipment. Although the DTS is completely self-testing, there are certain other verifications that may be made by using external test instruments.

Power supply voltages are non-adjustable. Accurate measurement of Power supplies can be made using a digital voltmeter. Test points (POSTS) are labeled on the bottom PC board for easy access.

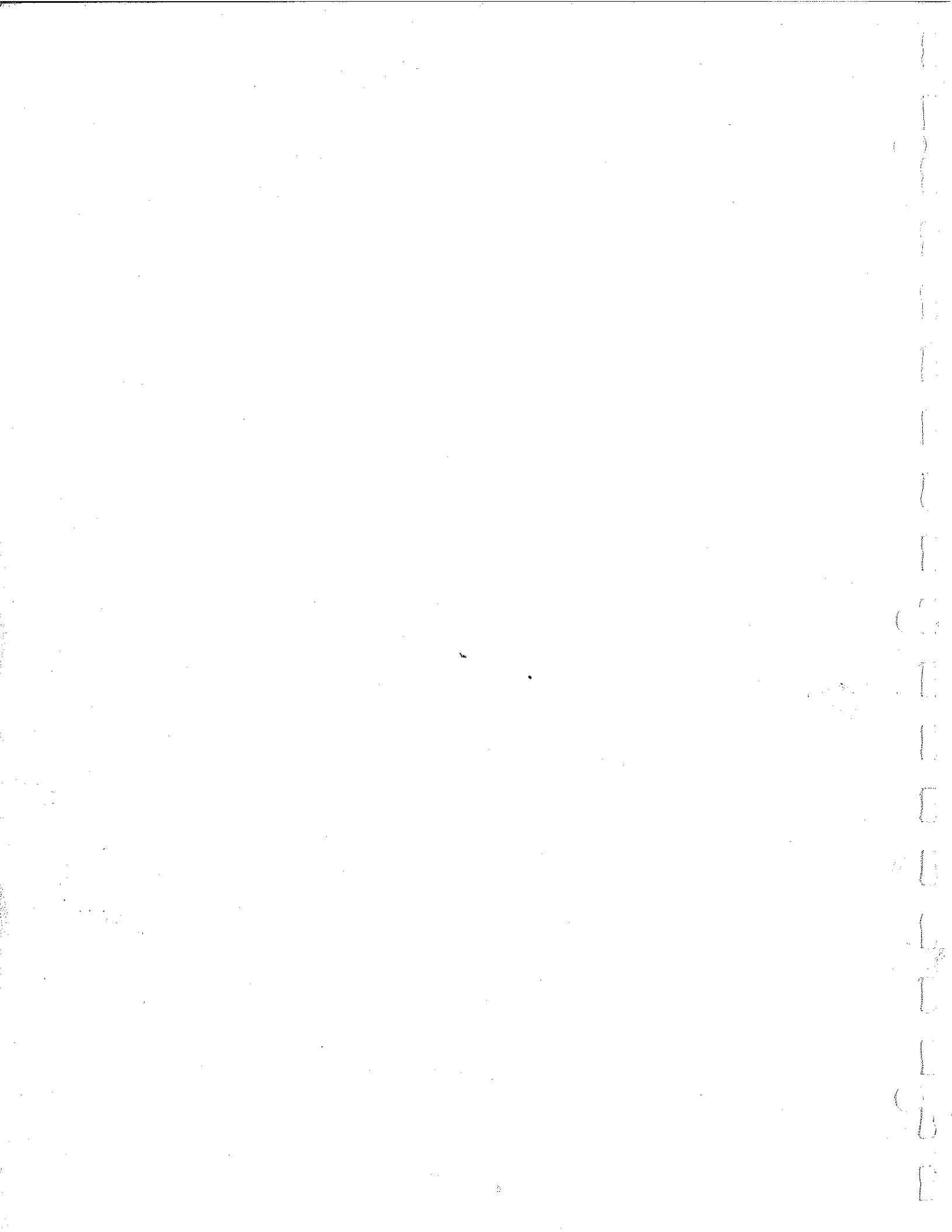
- +12 volts tolerance ± 10 percent
- -12 volts tolerance ± 10 percent
- +5 volts tolerance ± 10 percent

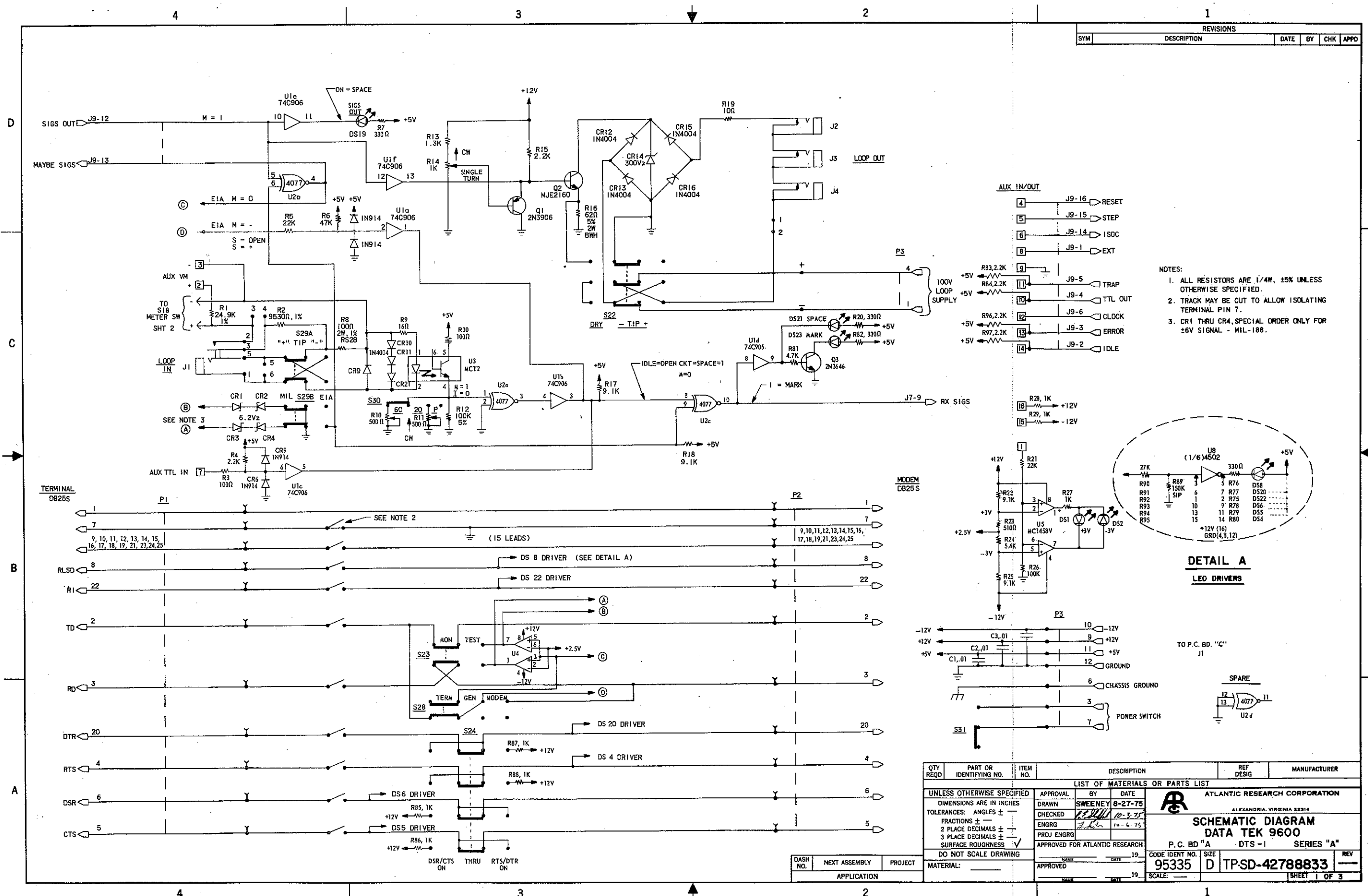
All Bit Rates are generated from a single crystal oscillator. An external frequency counter can be applied to the AUX CLOCK lead for a ± 12 -volt signal. The Frequency of the CLOCK is equal to the Bit Rate selected on the Panel.

TM 833

SECTION VI

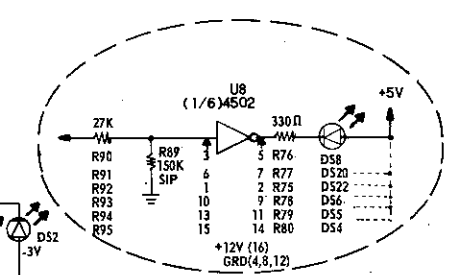
DRAWINGS



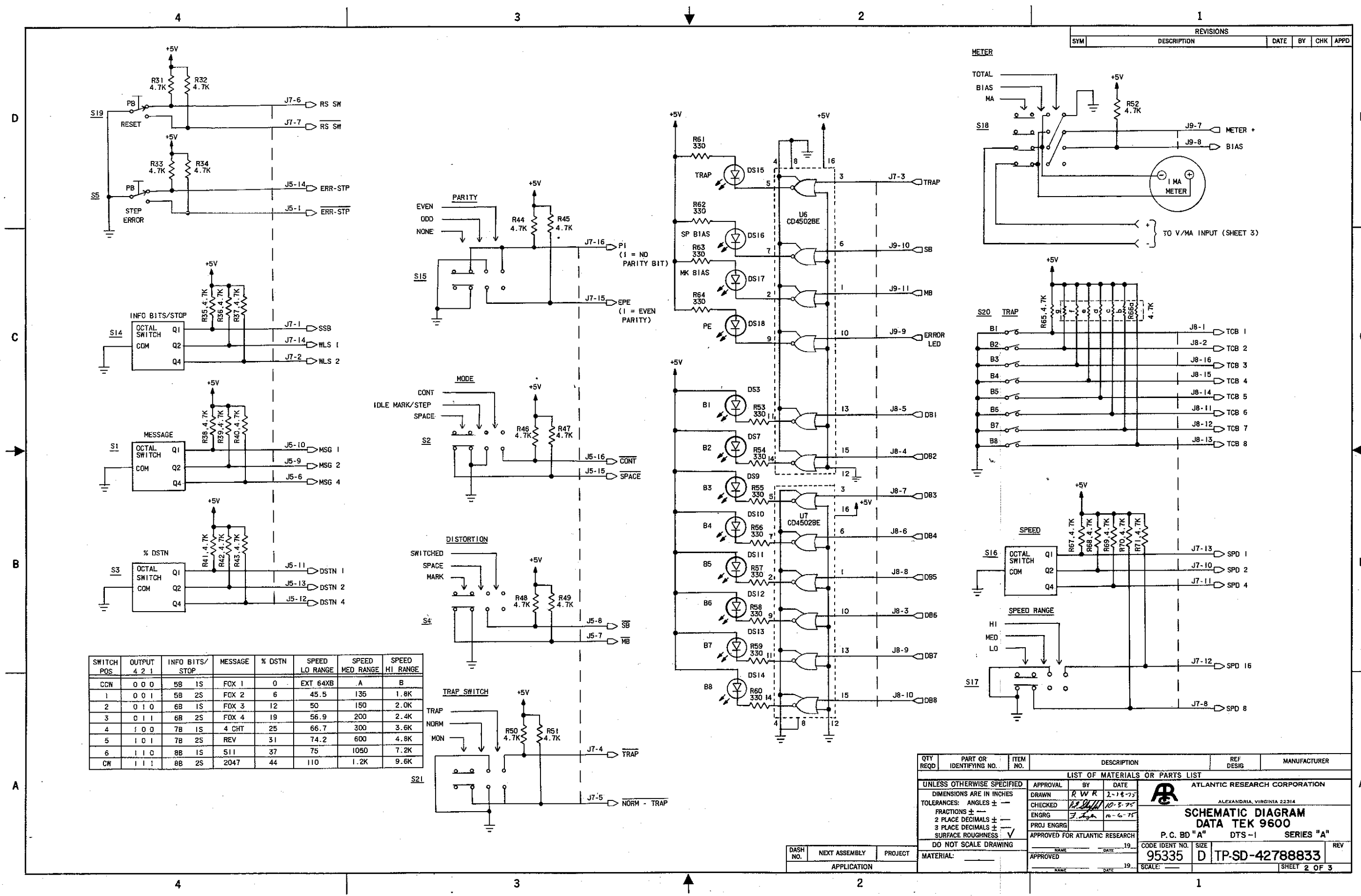


REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK	APPD

- NOTES:
1. ALL RESISTORS ARE 1/4W, ±5% UNLESS OTHERWISE SPECIFIED.
 2. TRACK MAY BE CUT TO ALLOW ISOLATING TERMINAL PIN 7.
 3. CR1 THRU CR4, SPECIAL ORDER ONLY FOR ±6V SIGNAL - MIL-188.

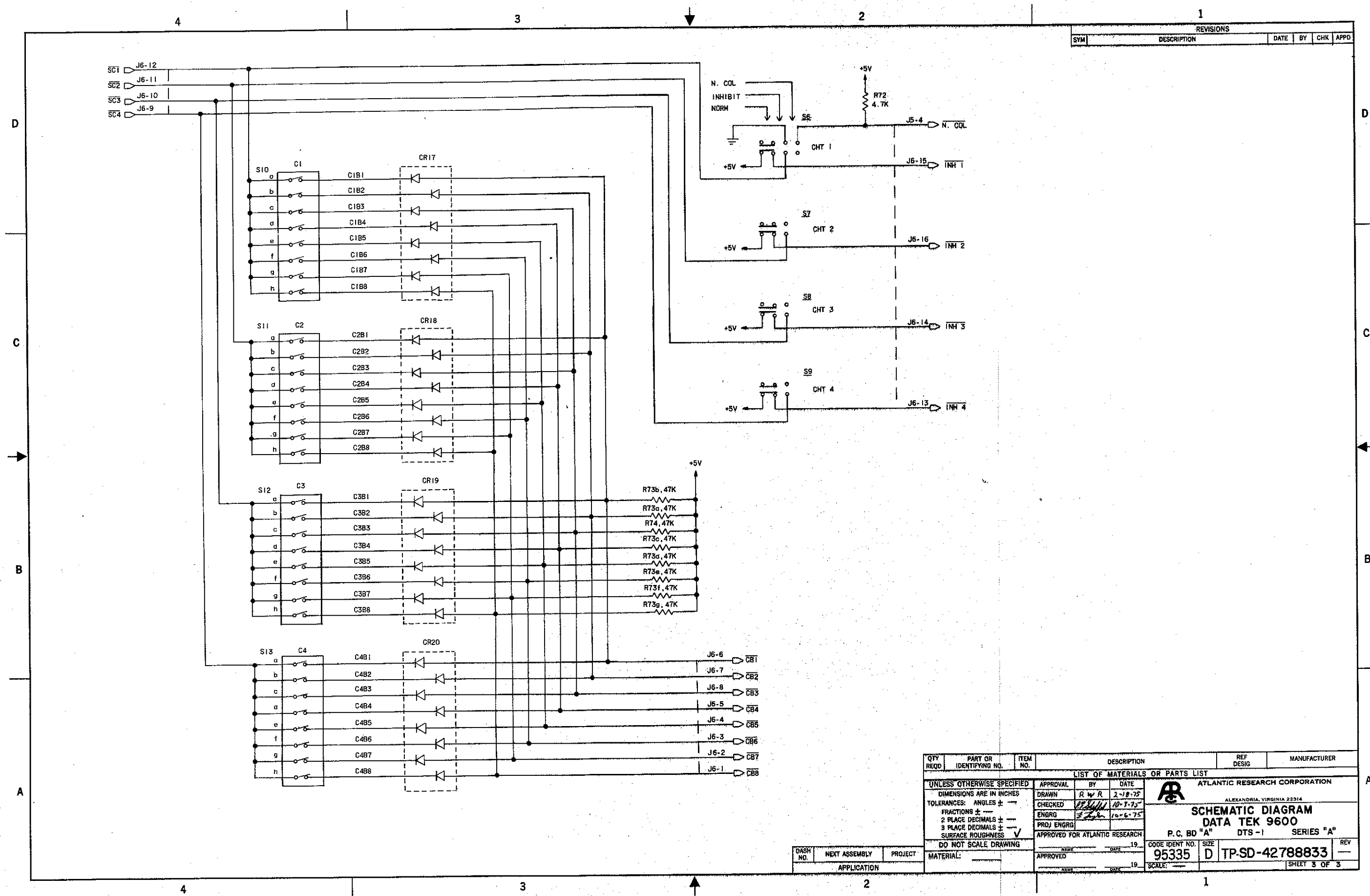


QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
LIST OF MATERIALS OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES					
TOLERANCES: ANGLES ±					
FRACTIONS ±					
2 PLACE DECIMALS ±					
3 PLACE DECIMALS ±					
SURFACE ROUGHNESS					
DO NOT SCALE DRAWING					
MATERIAL:					
APPROVED FOR ATLANTIC RESEARCH					
APPROVED					
ATLANTIC RESEARCH CORPORATION					
ALEXANDRIA, VIRGINIA 22314					
SCHEMATIC DIAGRAM					
DATA TEK 9600					
P.C. BD "A" DTS - I SERIES "A"					
CODE IDENT NO. 95335					
SIZE D					
TP-SD-42788833					
SCALE					
SHEET 1 OF 3					



SWITCH POS	OUTPUT 4 2 1	INFO BITS/ STOP	MESSAGE	% DSTN	SPEED LO RANGE	SPEED MED RANGE	SPEED HI RANGE
CCW	0 0 0	5B 1S	FOX 1	0	EXT 64XB	A	B
1	0 0 1	5B 2S	FOX 2	6	45.5	135	1.8K
2	0 1 0	6B 1S	FOX 3	12	50	150	2.0K
3	0 1 1	6B 2S	FOX 4	19	56.9	200	2.4K
4	1 0 0	7B 1S	4 CHT	25	66.7	300	3.6K
5	1 0 1	7B 2S	REV	31	74.2	600	4.8K
6	1 1 0	8B 1S	511	37	75	1050	7.2K
CW	1 1 1	8B 2S	2047	44	110	1.2K	9.6K

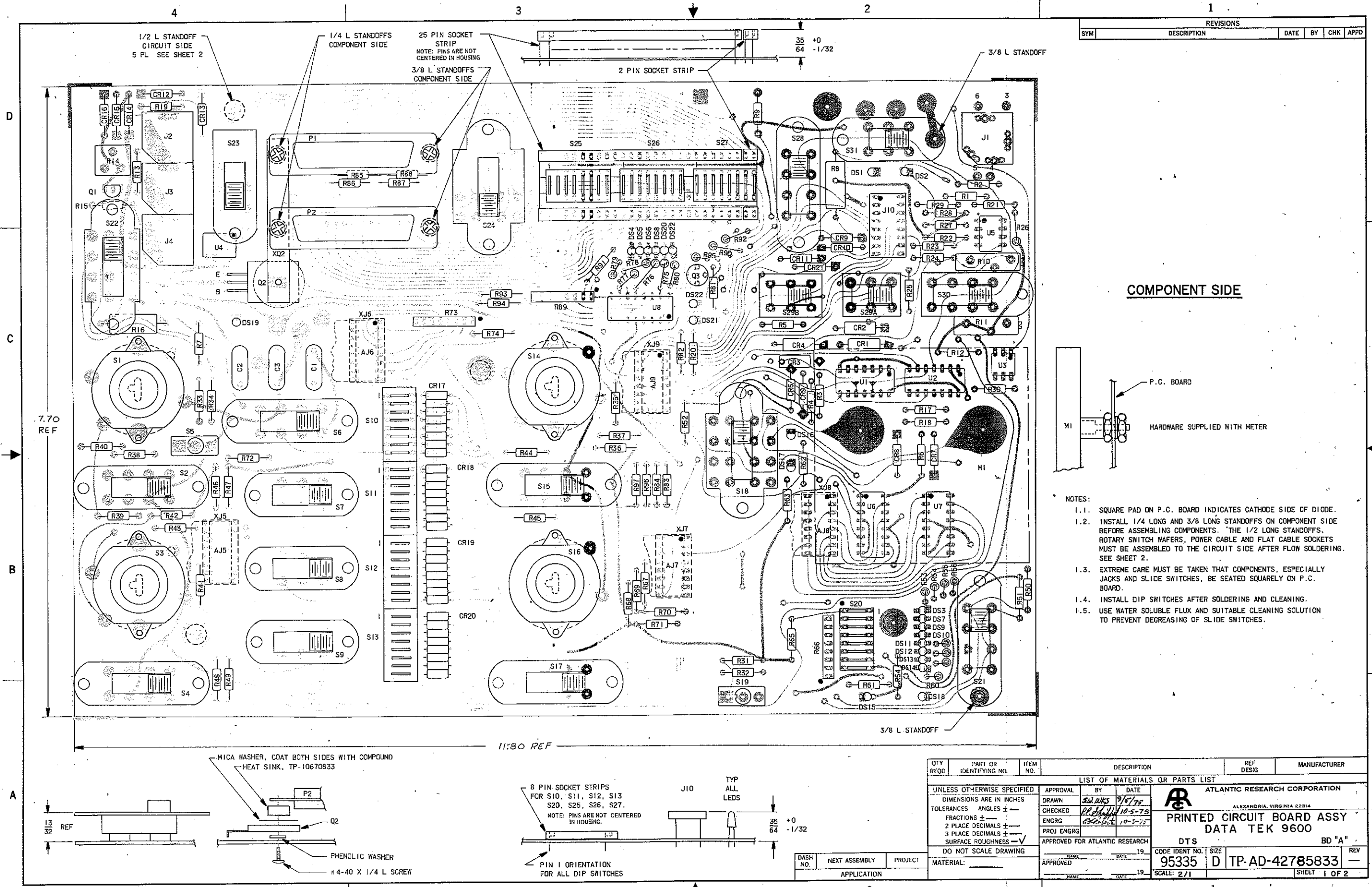
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TOLERANCES: ANGLES ±			DRAWN	RWR	2-18-75
FRACTIONS ±			CHECKED	J. J.	10-5-75
2 PLACE DECIMALS ±			ENGRG	J. J.	10-6-75
3 PLACE DECIMALS ±			PROJ ENGRG		
SURFACE ROUGHNESS			APPROVED FOR ATLANTIC RESEARCH		
DO NOT SCALE DRAWING			NAME	DATE	19
MATERIAL:			APPROVED	NAME	DATE
DASH NO.			NEXT ASSEMBLY	PROJECT	APPLICATION
ATLANTIC RESEARCH CORPORATION			ALEXANDRIA, VIRGINIA 22314		
SCHEMATIC DIAGRAM			DATA TEK 9600		
P.C. BD "A"			DTS-I		
SERIES "A"					
CODE IDENT NO.			SIZE	SCALE	REV
95335			D	TP-SD-42788833	
SHEET 2 OF 3					



REVISIONS				
SYM	DESCRIPTION	DATE	BY	CHK APPD

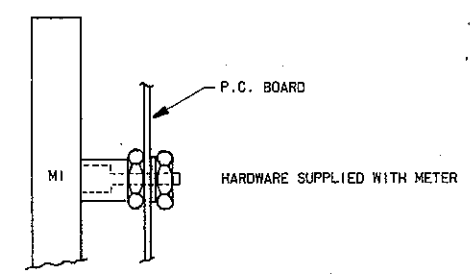
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TOLERANCES: ANGLES ±			CHECKED	10-1-75	
FRACTIONS ±			ENGRG	10-6-75	
2 PLACE DECIMALS ±			PROJ/ ENGRG		
3 PLACE DECIMALS ±			APPROVED FOR ATLANTIC RESEARCH		
SURFACE ROUGHNESS			DO NOT SCALE DRAWING		
MATERIAL:			APPROVED		
DASH NO.	NEXT ASSEMBLY	PROJECT	DATE	19	
APPLICATION			DATE	19	
			SCALE:		
			CODE IDENT NO.	SIZE	REV
			95335	D	
			TP-SD-42788833		
			SHEET 3 OF 3		

ATLANTIC RESEARCH CORPORATION
ALEXANDRIA, VIRGINIA 22314
SCHEMATIC DIAGRAM
DATA TEK 9600
P.C. BD "A" DTS-1 SERIES "A"

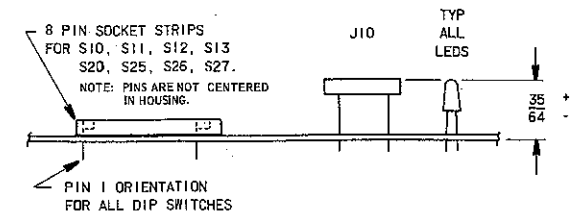
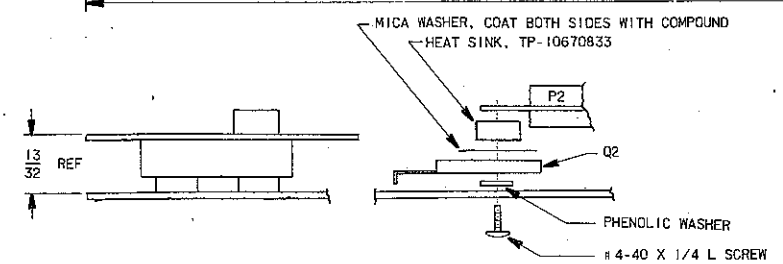


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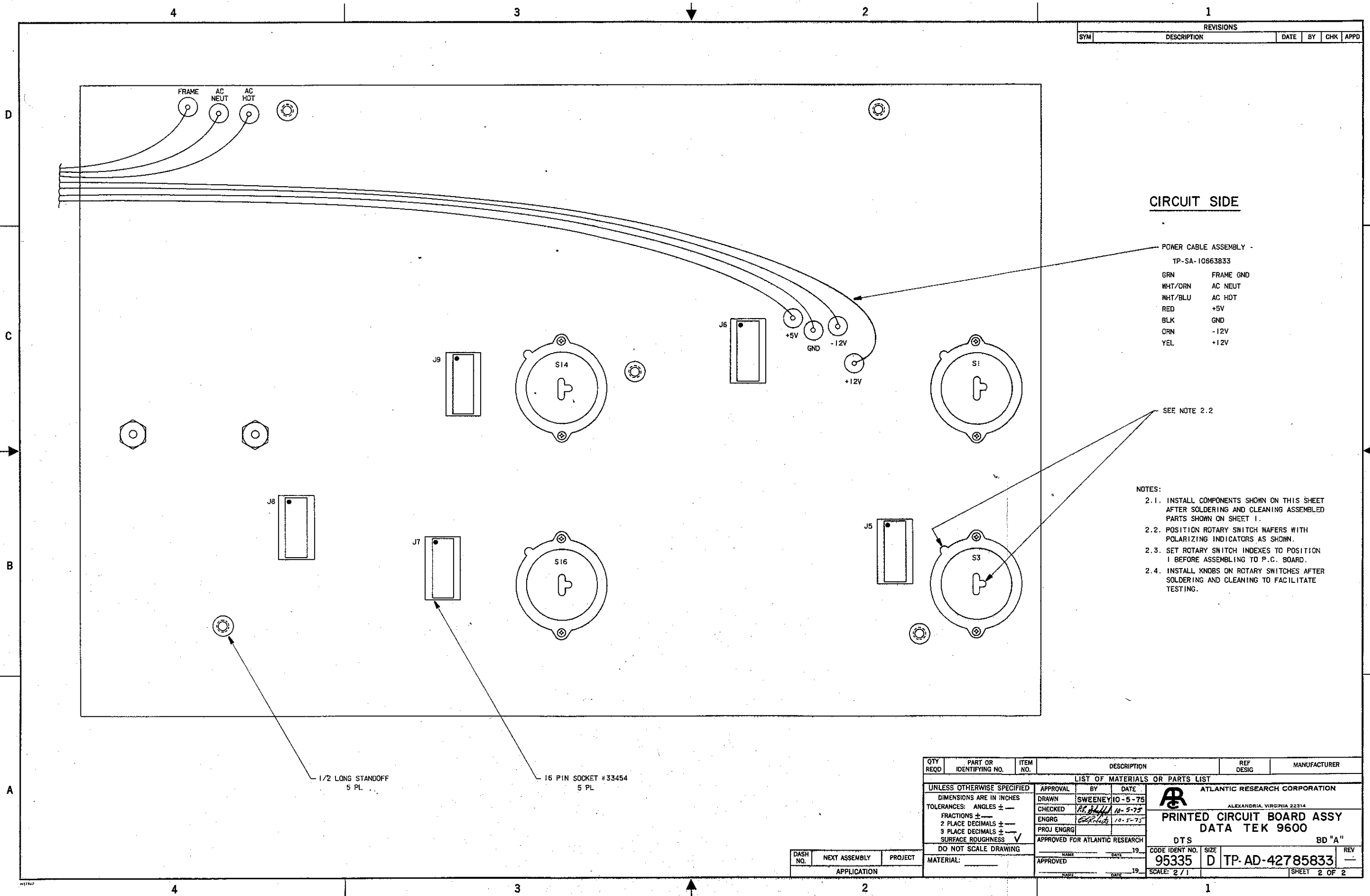
COMPONENT SIDE



- NOTES:
- 1.1. SQUARE PAD ON P.C. BOARD INDICATES CATHODE SIDE OF DIODE.
 - 1.2. INSTALL 1/4 LONG AND 3/8 LONG STANDOFFS ON COMPONENT SIDE BEFORE ASSEMBLING COMPONENTS. THE 1/2 LONG STANDOFFS, ROTARY SWITCH WAFERS, POWER CABLE AND FLAT CABLE SOCKETS MUST BE ASSEMBLED TO THE CIRCUIT SIDE AFTER FLOW SOLDERING. SEE SHEET 2.
 - 1.3. EXTREME CARE MUST BE TAKEN THAT COMPONENTS, ESPECIALLY JACKS AND SLIDE SWITCHES, BE SEATED SQUARELY ON P.C. BOARD.
 - 1.4. INSTALL DIP SWITCHES AFTER SOLDERING AND CLEANING.
 - 1.5. USE WATER SOLUBLE FLUX AND SUITABLE CLEANING SOLUTION TO PREVENT DEGREASING OF SLIDE SWITCHES.

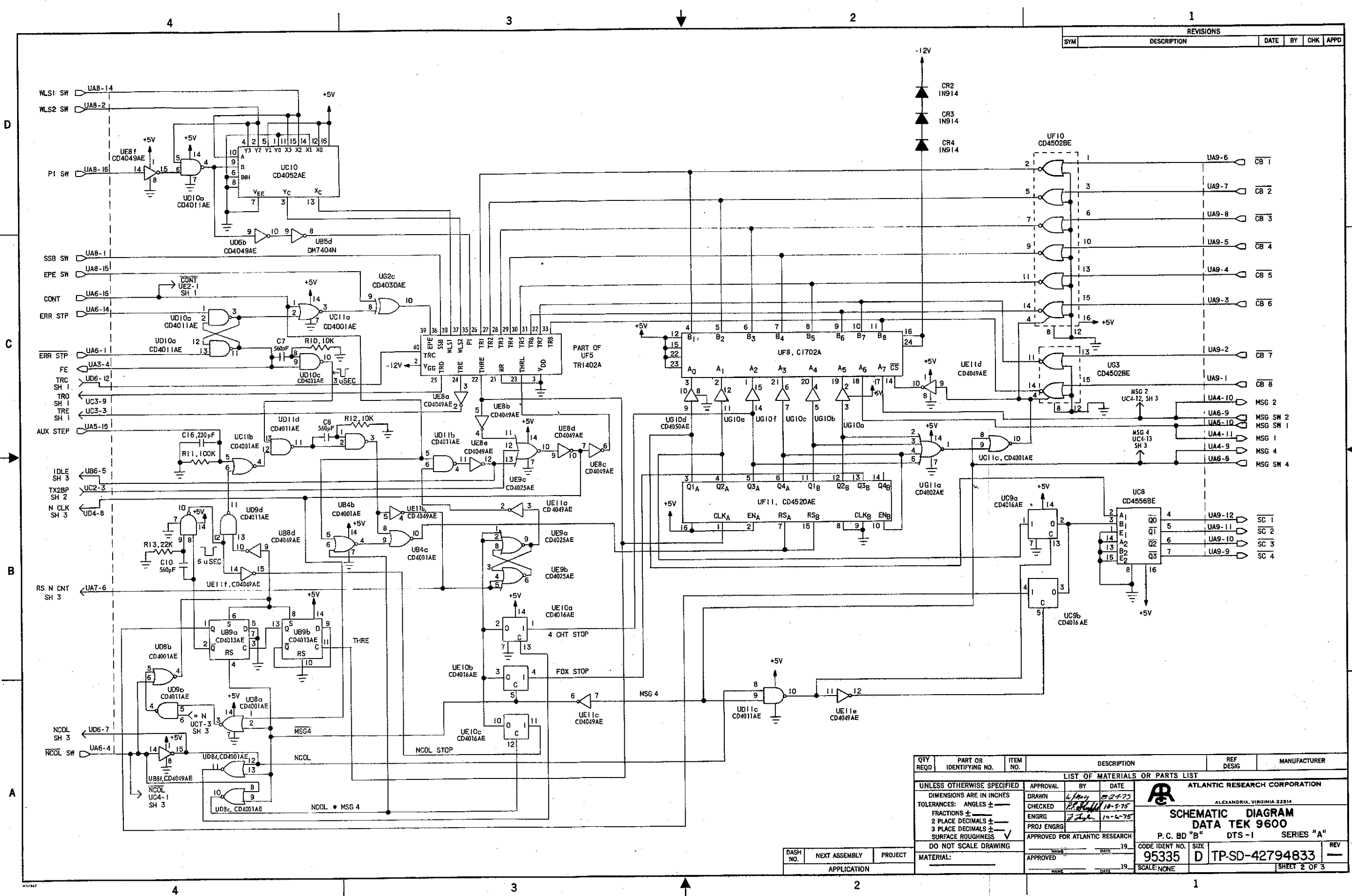


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UNLESS OTHERWISE SPECIFIED								
DIMENSIONS ARE IN INCHES			APPROVAL	BY	DATE			
TOLERANCES ANGLES ±			DRAWN	SW/MS	9/5/75			
FRACTIONS ±			CHECKED	RE/MS	10-5-75			
2 PLACE DECIMALS ±			ENGRG	6/4/75	10-5-75			
3 PLACE DECIMALS ±			PROJ ENGRG					
SURFACE ROUGHNESS - V			APPROVED FOR ATLANTIC RESEARCH					
DO NOT SCALE DRAWING			NAME	DATE	19			
MATERIAL:			APPROVED	DATE	19			
DASH NO.			NEXT ASSEMBLY PROJECT APPLICATION					
ATLANTIC RESEARCH CORPORATION								
ALEXANDRIA, VIRGINIA 22314								
PRINTED CIRCUIT BOARD ASSY								
DATA TEK 9600								
DTS								
BD "A"								
CODE IDENT NO.			SIZE					
95335			D TP-AD-42785833					
SCALE: 2/1			SHEET 1 OF 2					



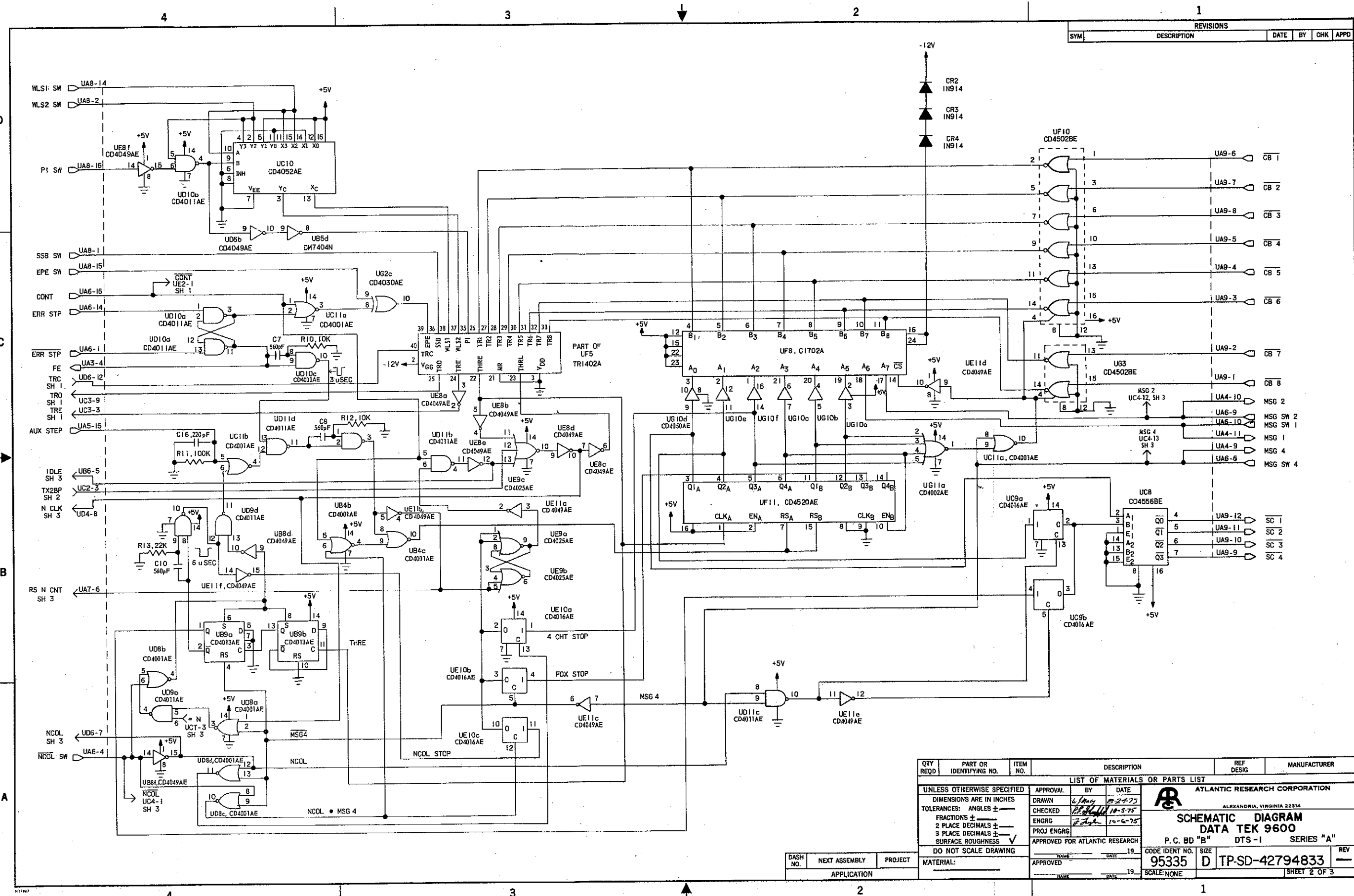
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UNLESS OTHERWISE SPECIFIED			APPROVAL	BY	DATE
DIMENSIONS ARE IN INCHES			DRAWN	SWEENEY	10-5-75
TOLERANCES: ANGLES ±			CHECKED	PE	10-5-75
FRACTIONS ±			ENGRG	CR	10-5-75
2 PLACE DECIMALS ±			PROJ ENGRG		
3 PLACE DECIMALS ±			APPROVED FOR ATLANTIC RESEARCH		
SURFACE ROUGHNESS ✓			APPROVED		
DO NOT SCALE DRAWING			NAME	DATE	19
MATERIAL:			NAME	DATE	19
DASH NO.	NEXT ASSEMBLY	PROJECT	APPLICATION		
			NAME	DATE	19

ATLANTIC RESEARCH CORPORATION	
ALEXANDRIA, VIRGINIA 22314	
PRINTED CIRCUIT BOARD ASSY	
DATA TEK 9600	
DTS	BD "A"
CODE IDENT NO.	SIZE
95335	D
TP-AD-42785833	REV
SCALE: 2 / 1	SHEET 2 OF 2

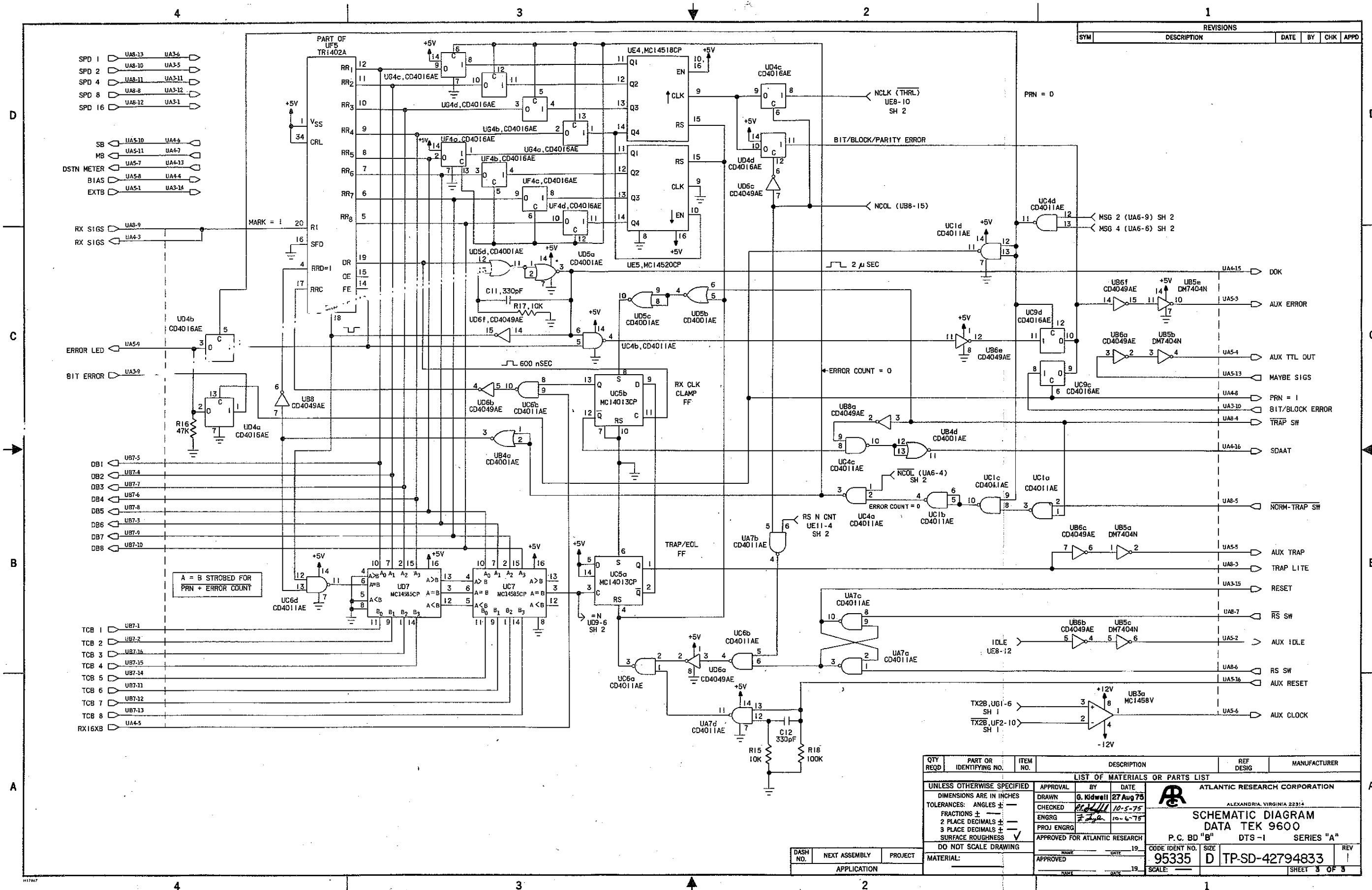


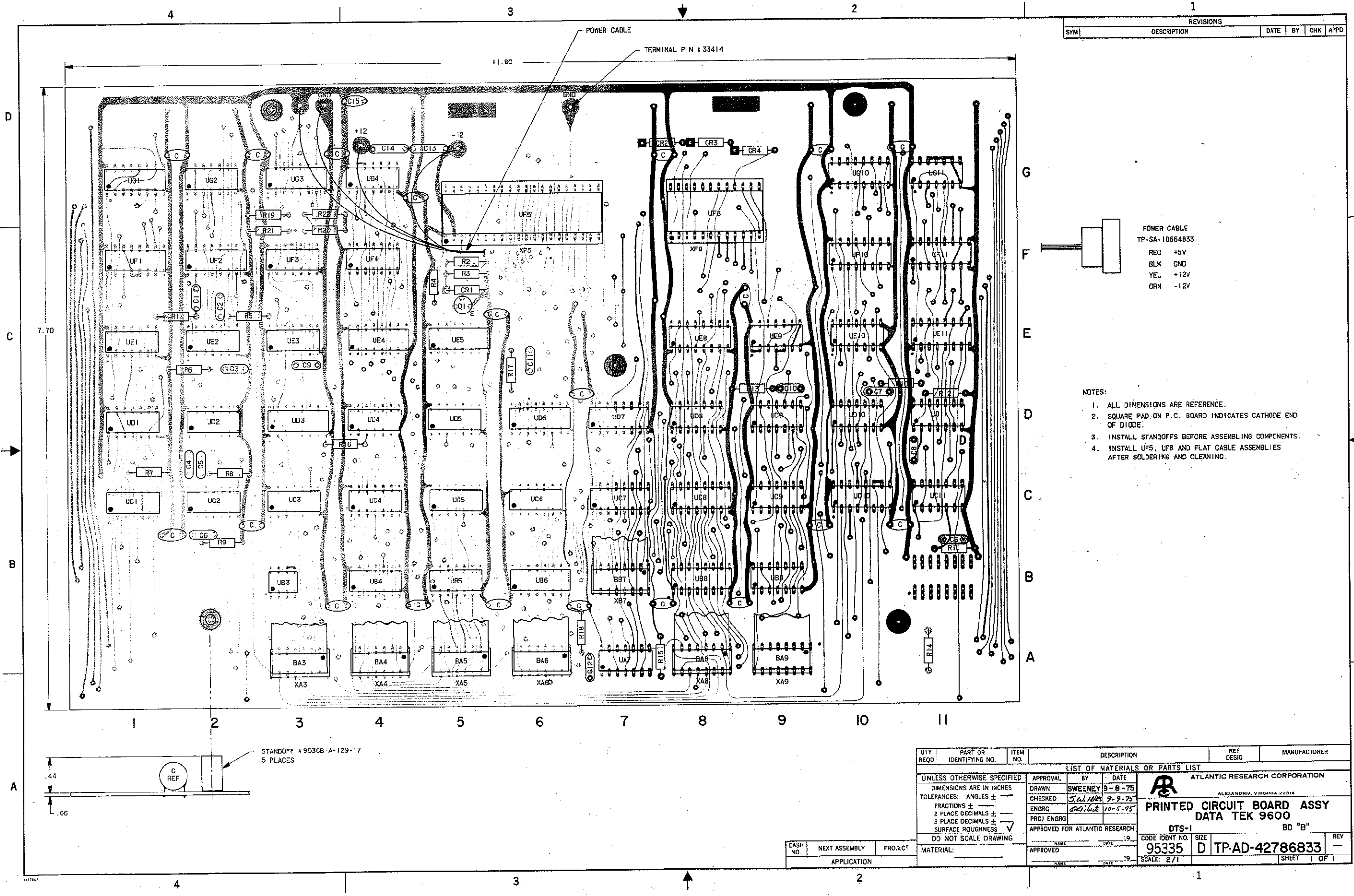
REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK	APPD

QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES			APPROVAL	BY	DATE
TOLERANCES: ANGLES ±			DRAWN	6/10/75	5-24-75
FRACTIONS ±			CHECKED	6/10/75	10-5-75
2 PLACE DECIMALS ±			ENGRG	6/10/75	10-5-75
3 PLACE DECIMALS ±			PROJ ENGRG		
SURFACE ROUGHNESS			APPROVED FOR ATLANTIC RESEARCH		
DO NOT SCALE DRAWING			APPROVED		
MATERIAL:			APPROVED		
DASH NO.			NEXT ASSEMBLY		
PROJECT			APPLICATION		
ATLANTIC RESEARCH CORPORATION			ALEXANDRIA, VIRGINIA 22314		
SCHEMATIC DIAGRAM			DATA TEK 9600		
P.C. BD "B"			DTS -1		
CODE IDENT NO.			SIZE		
95335			D		
TP-SD-42794833			REV		
SCALE: NONE			SHEET 2 OF 3		

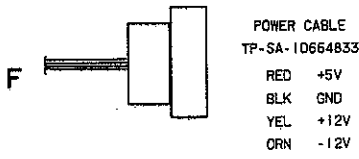


QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
LIST OF MATERIALS OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES	DRAWN	BY	DATE	ATLANTIC RESEARCH CORPORATION	
TOLERANCES: ANGLES ±	CHECKED	DATE	10-5-75	ALEXANDRIA, VIRGINIA 22314	
FRACTIONS ±	ENGRG	DATE	10-6-75	SCHEMATIC DIAGRAM	
2 PLACE DECIMALS ±	PROJ ENGRG	DATE		DATA TEK 9600	
3 PLACE DECIMALS ±	APPROVED FOR ATLANTIC RESEARCH	DATE	19	P.C. BD "B" DTS-1 SERIES "A"	
SURFACE ROUGHNESS	APPROVED	DATE	19	CODE IDENT NO. SIZE	
DO NOT SCALE DRAWING				95335 D TP-SD-42794833	
MATERIAL:				SCALE: NONE	
				SHEET 2 OF 3	





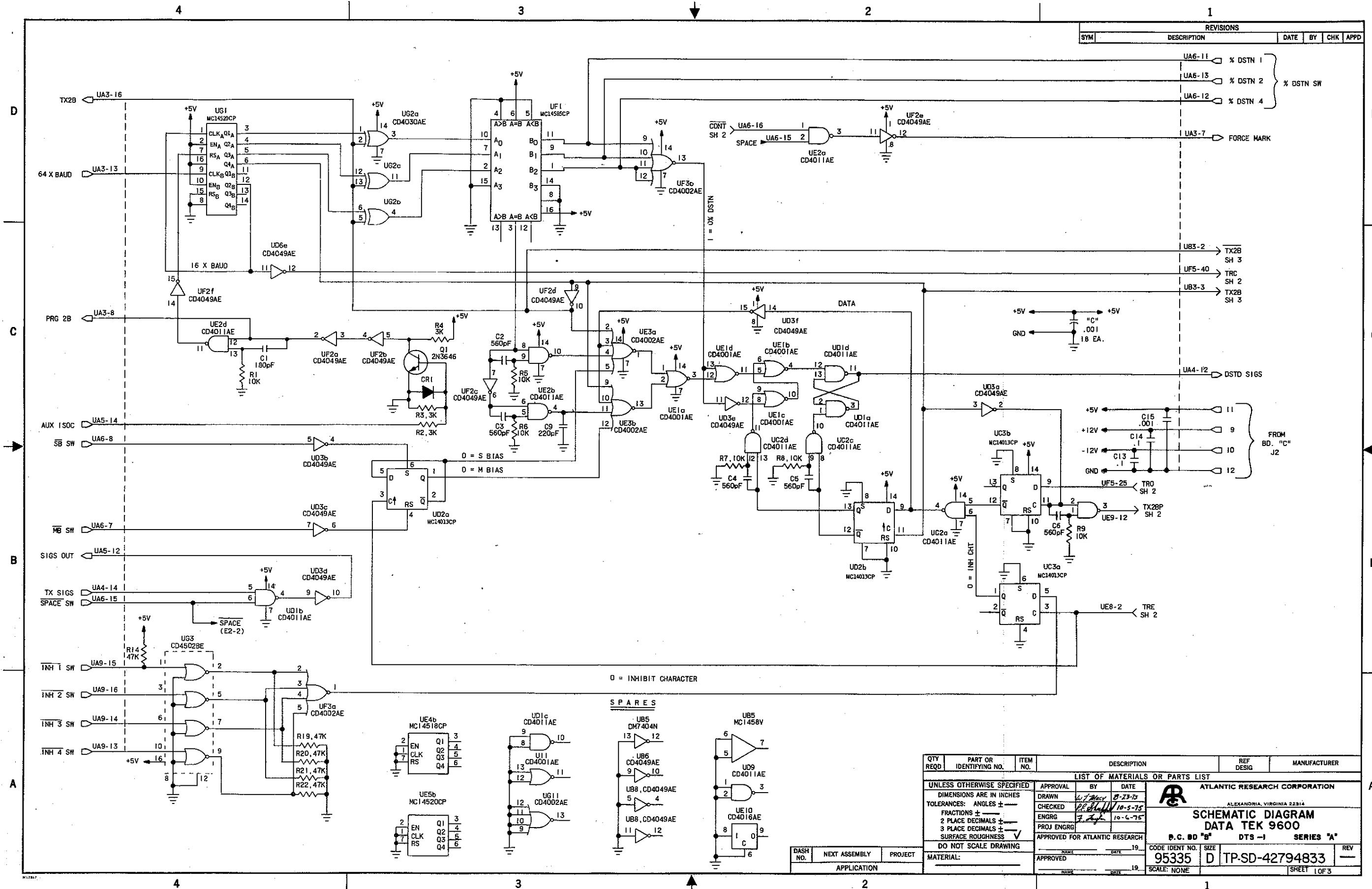
REVISIONS				
SYM	DESCRIPTION	DATE	BY	CHK APPD

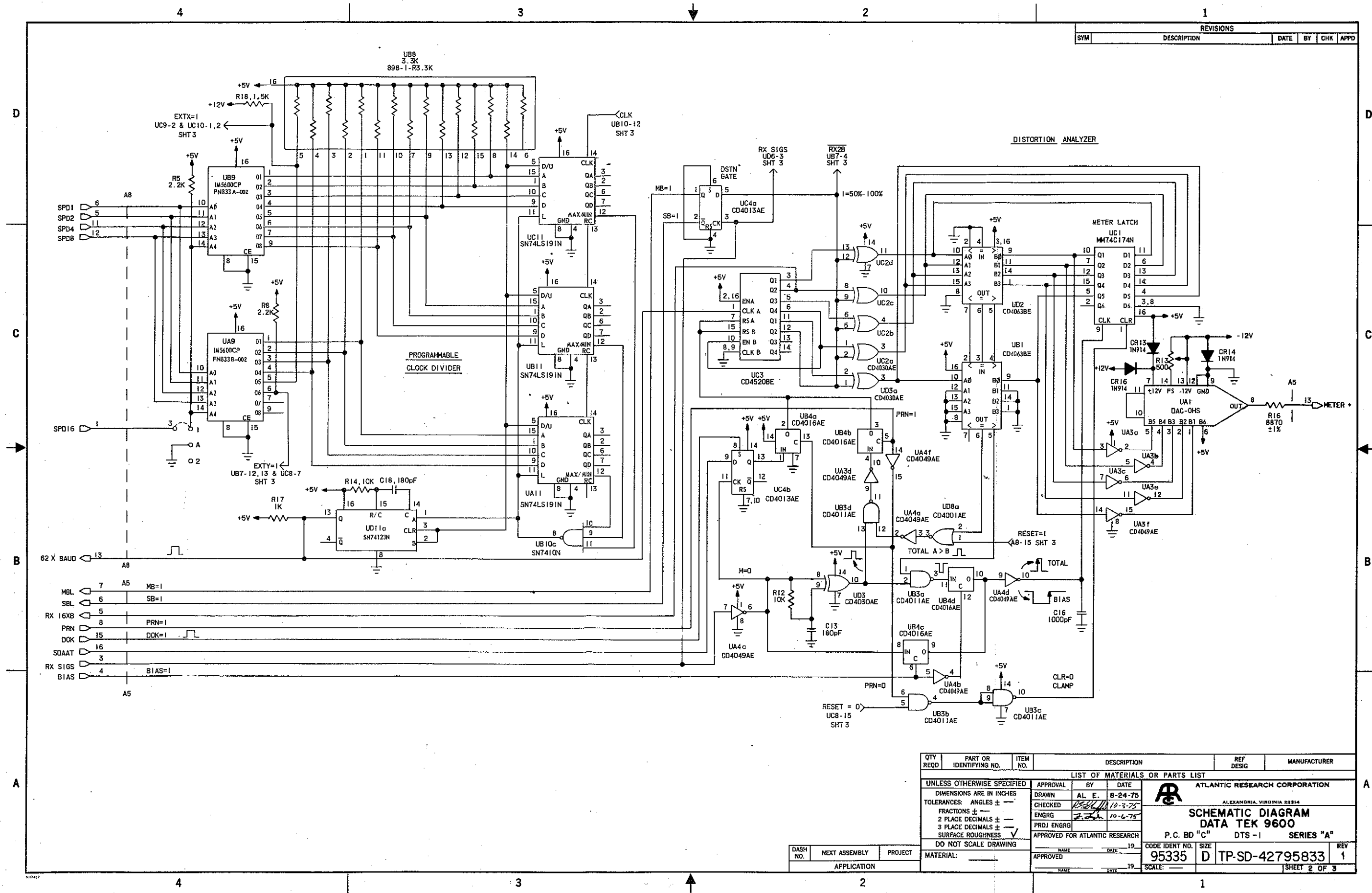


- NOTES:
1. ALL DIMENSIONS ARE REFERENCE.
 2. SQUARE PAD ON P.C. BOARD INDICATES CATHODE END OF DIODE.
 3. INSTALL STANDOFFS BEFORE ASSEMBLING COMPONENTS.
 4. INSTALL UF5, UF8 AND FLAT CABLE ASSEMBLIES AFTER SOLDERING AND CLEANING.

QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
LIST OF MATERIALS OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED			APPROVAL	BY	DATE
DIMENSIONS ARE IN INCHES			DRAWN	SWEENEY	9-8-75
TOLERANCES: ANGLES ±			CHECKED	5.6.1.10.15	9-9-75
FRACTIONS ±			ENGRG	6.9.1.14.16	10-5-75
2 PLACE DECIMALS ±			PROJ ENGRG		
3 PLACE DECIMALS ±					
SURFACE ROUGHNESS					
DO NOT SCALE DRAWING			APPROVED FOR ATLANTIC RESEARCH		
MATERIAL:			NAME	DATE	19
DASH NO.			APPROVED	NAME	DATE
NEXT ASSEMBLY			PROJECT		
APPLICATION					

ATLANTIC RESEARCH CORPORATION	
ALEXANDRIA, VIRGINIA 22314	
PRINTED CIRCUIT BOARD ASSY	
DATA TEK 9600	
DTS-1	BD "B"
CODE IDENT NO.	SIZE
95335	D
SCALE: 2/1	TP-AD-42786833
SHEET 1 OF 1	REV



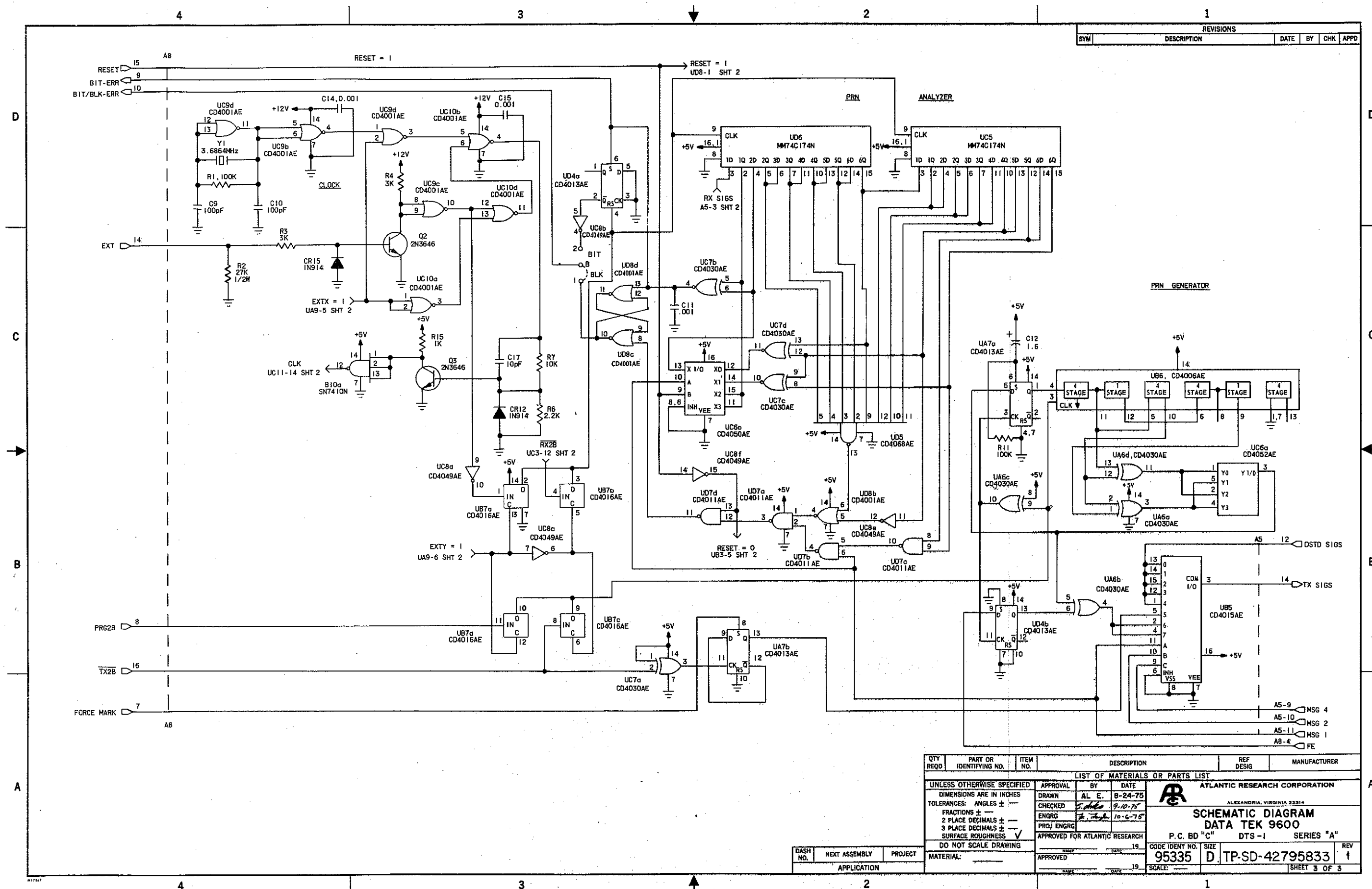


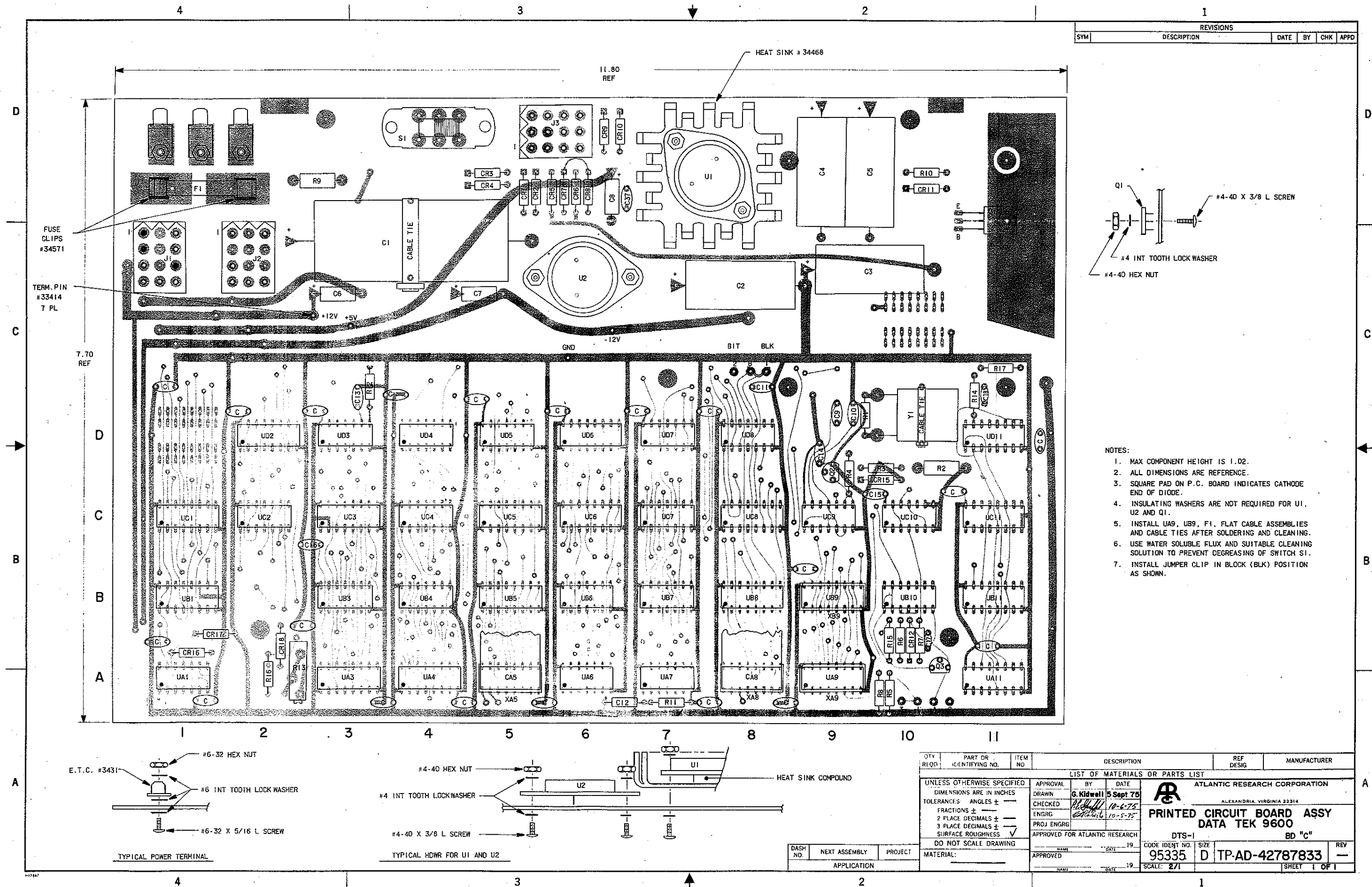
REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK	APPD

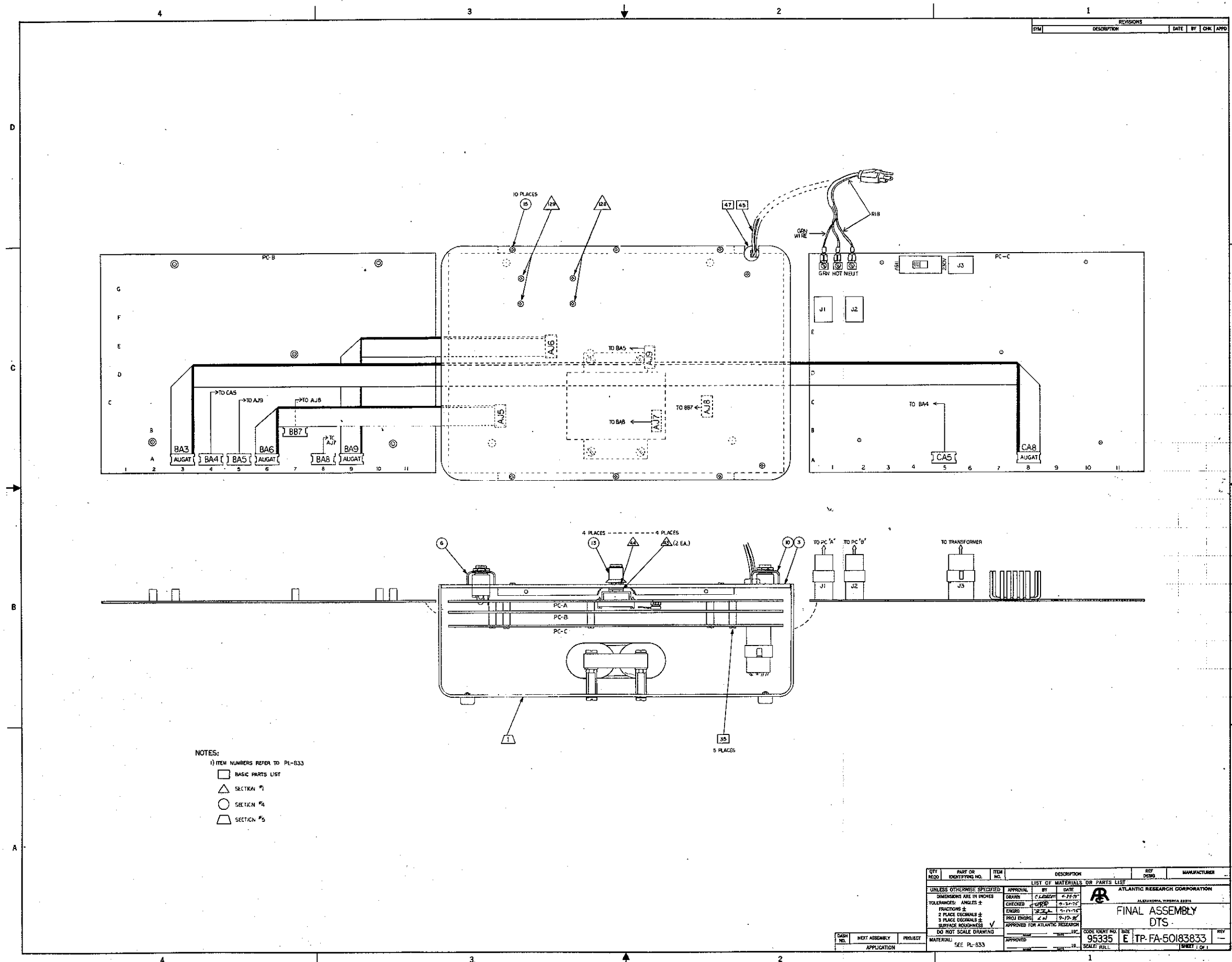
DISTORTION ANALYZER

QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
LIST OF MATERIALS OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED			APPROVAL	BY	DATE
DIMENSIONS ARE IN INCHES			DRAWN	AL E.	8-24-75
TOLERANCES: ANGLES ±			CHECKED	10-3-75	
FRACTIONS ±			ENGRG	10-6-75	
2 PLACE DECIMALS ±			PROJ ENGRG		
3 PLACE DECIMALS ±			APPROVED FOR ATLANTIC RESEARCH		
SURFACE ROUGHNESS			DO NOT SCALE DRAWING		
MATERIAL:			NAME	DATE	19
DASH NO.			APPROVED	NAME	DATE
NEXT ASSEMBLY			CODE IDENT NO.	SIZE	REV
PROJECT			95335	D	1
APPLICATION			SCALE		

ATLANTIC RESEARCH CORPORATION
ALEXANDRIA, VIRGINIA 22314
SCHEMATIC DIAGRAM
DATA TEK 9600
P.C. BD "C" DTS-1 SERIES "A"
95335 D TP-SD-42795833
SHEET 2 OF 3







TM 833

APPENDIX

ADDENDUM

ISOC: Brief Description

Basically ISOChronous transmission uses a character bit structure including one start and any multiple of unit stop elements. Each bit is released from the data source in phase with a clock provided by the transmission facilities. The negative transition of the clock occurs in the *middle* of the Data Bit.

ISOC deviates from ASYNC in that ASYNC permits variable stop bit (idle) periods. Timing constraints apply only to the start bit and the data bits. No clock lead is associated with ASYNC.

ISOC deviates from SYNC in that SYNC characters use only data bits (no start or stop elements). SYNC also requires a separate clock lead to establish timing for all bits. SYNC also requires character synchronization by preceding each message with 2 or more SYN characters.

An ISOC receiver usually ignores the clock lead and treats the signal as an ASYNC signal.

The DATA-TEK is operated as an ISOC signal source by connecting the transmission interface transmit clock output (SCT pin 15) to the AUX ISOC input. Unit stop bits must be selected for Data Format. The DATA-TEK BIT RATE must be selected to agree with transmission link bit rate in order to accurately generate Distortion.

HEX TO CHARACTER CODE FOR DATA COMMUNICATIONS

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7-BIT ASCII	EBCDIC		SELECTRIC	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7-BIT ASCII	EBCDIC		SELECTRIC
				UC	LC						UC	LC	
00 NUL	NUL		00 NUL				40 SP		@	40 @	SP	SP	
01 SOH		SOH	01 SOH			O I	41	A		41 A			
02 STX		STX	02 STX	e	@	T t	42	B		42 B			
03 ETX	ETX		03 ETX				43		C	43 C	+	&	J j
04 PF		EOT	04 EOT	*	8	\$ 4	44	D		44 D			
05 HT	ENQ		05 ENQ				45		E	45 E	Q	q	O o
06 LC	ACK		06 ACK				46		F	46 F	Y	y	L l
07 DEL		BEL	07 BEL	H	h	? 1	47	G		47 G			
08		BS	08 BS	:	4	% 5	48	H		48 H			
09 RLF	HT		09 HT				49		I	49 I	M	m	" "
0A SMM	LF		0A LF				4A		J	4A J			E e
0B VT		VT	0B VT	D	d	P p	4B	K		4B K	U	u	
0C FF	FF		0C FF				4C		L	4C L	PN		PN
0D CR		CR	0D CR	RES		RES	4D	M		4D M			
0E SO		SO	0E SO	BYP		BY	4E	N		4E N			
0F SI	SI		0F SI				4F		O	4F O	PF		PF
10 DLE		DLE	10 DLE	<	2	@ 2	50	P		50 P			
11 DC1	DC1		11 DC1				51		Q	51 Q	K	k	• •
12 DC2	DC2		12 DC2				52		R	52 R	S	s	N n
13 DC3		DC3	13 DC3	B	b	+ =	53	S		53 S			
14 RES	DC4		14 DC4				54		T	54 T	)	0	Z z
15 NL		NAK	15 NAK				55	U		55 U			
16 BS		SYN	16 SYN				56	V		56 V			
17 IL	ETB		17 ETB				57		W	57 W			
18 CAN	CAN		18 CAN				58		X	58 X	6		e 6
19 EM		EM	19 EM	O	o	I i	59	Y		59 Y			
1A CC		SUB	1A SUB	W	w	K k	5A	Z		5A Z			
1B	ESC		1B ESC				5B			5B	F	f	Q q
1C IFS		FS	1C FS	UPPER		UPPER	5C	\	\	5C \			
1D IGS	GS		1D GS	CASE		CASE	5D		}	5D }	BS		BS
1E IRS	RS		1E RS				5E		^	5E ^	EOB		EOB
1F IUS		US	1F US	LOWER		LOWER	5F	—	—	5F —			
20 DS		SP	20 SP	=	1	[z] 1	60			60			
21 SOS	!		21 !				61		a	61 a	J	j	M m
22 FS	"		22 "				62		b	62 b	?	/	X x
23		#	23 #	A	a	G g	63	c		63 c			
24 BYP	\$		24 \$				64		d	64 d	(	9	) 0
25 LF		%	25 %	R	r	S s	65	e		65 e			
26 EOB/ETB		&	26 &	Z	z	H h	66	f		66 f			
27 ESC/PRE			27				67		g	67 g	I	i	Y y
28	(		28 (				68		h	68 h	%	5	& 7
29	)		29)	N	n	R r	69	i		69 i			
2A SM	*		2A *	V	v	D d	6A	j		6A j			
2B	+		2B +				6B		k	6B k	E	e	:
2C			2C	RS		RS	6C	l		6C l			
2D ENQ	—		2D —				6D	m		6D m	NL		NL
2E ACK	.		2E .				6E	n		6E n	LF		LF
2F BEL	/		2F /	HT		HT	6F	o		6F o			
30	0		30 0	:	3		70		p	70 p			# 3
31		1	31 1	L	l	V v	71	q		71 q			
32 SYN		2	32 2	T	t	U u	72	r		72 r			
33	3		33 3				73		s	73 s	C	c	F f
34 PN		4	34 4	"	#	(9	74	t		74 t			
35 RS	5		35 5				75		u	75 u	!	\$	W w
36 UC	6		36 6				76		v	76 v	i	.	B b
37 EOT		7	37 7	—		—	77	w		77 w			
38		8	38 8	>	7	* 8	78	x		78 x			
39	9		39 9				79	y		79 y	P	p	A a
3A	:		3A :				7A	z		7A z	X	x	C c
3B			3B	G	g		7B			7B			
3C DC4	<		3C <				7C	@		7C	EOT		EOT
3D NAK		=	3D =	IL		IL	7D			7D			
3E		>	3E >	PRE		PRE	7E	=		7E			
3F SUB	?		3F ?				7F		DEL	7F DEL	DEL		DEL



COURTESY OF

ATLANTIC RESEARCH CORPORATION

5390 CHEROKEE AVENUE ALEXANDRIA, VIRGINIA 22314

703-354-3400

MANUFACTURERS OF INTERSHAKE and DATA TEK 9600

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII		FIELD DATA	6-BIT TYPESETTER		6-BIT TRANSCODE	BAUDOT	
										SHIFT	UNSHIFT		LTRS	FIGS
80		NUL	NUL	C0 {	@	A	@		00			SOH		
81 a	SOH		SOH	C1 A			A		01 &	E	e	A	E	3
82 b	STX		STX	C2 B		B	B		02 ^	ELEVATE		B	LF	
83 c		ETX	ETX	C3 C	C		C		03	A	a	C	A	
84 d	EOT		EOT	C4 D		D	D		04	SPACE		D	SP	
85 e		ENQ	ENQ	C5 E	E		E		05 SP	S	s	E	S	BEL
86 f		ACK	ACK	C6 F	F		F		06 A	I	i	F	I	8
87 g	BEL		BEL	C7 G		G	G		07 B	U	u	G	U	7
88 h	BS		BS	C8 H		H	H		08 C	RETURN		H	CR	
89 i		HT	HT	C9 I	I		I		09 D	D	d	I	D	\$
8A		LF	LF	CA	J		J		0A E	R	r	STX	R	4
8B	VT		VT	CB		K	K		0B F	J	j		J	
8C		FF	FF	CC	L		L		0C G	N	n	<	N	
8D	CR		CR	CD		M	M		0D H	F	f	BELL	F	!
8E	SO		SO	CE		N	N		0E I	C	c	SUB	C	:
8F		SI	SI	CF	O		O		0F J	K	k	ETB	K	{
90	DLE		DLE	D0 }		P	P		10 K	T	t	&	T	5
91 j		DC1	DC1	D1 J	Q		Q		11 L	Z	z	J	Z	"
92 k		DC2	DC2	D2 K	R		R		12 M	L	l	K	L	}
93 l	DC3		DC3	D3 L		S	S		13 N	W	w	L	W	2
94 m		DC4	DC4	D4 M	T		T		14 O	H	h	M	H	#
95 n	NAK		NAK	D5 N		U	U		15 P	Y	y	N	Y	6
96 o	SYN		SYN	D6 O		V	V		16 Q	P	p	O	P	0
97 p		ETB	ETB	D7 P	W		W		17 R	Q	q	P	Q	1
98 q		CAN	CAN	D8 Q	X		X		18 S	O	o	Q	O	9
99 r	EM		EM	D9 R		Y	Y		19 T	B	b	R	B	?
9A	SUB		SUB	DA		Z	Z		1A U	G	g	SPACE	G	8
9B		ESC	ESC	DB	[		[		1B V	SHIFT		\$	FIGS	
9C	FS		FS	DC	\		\		1C W	M	m	*	M	.
9D		GS	GS	DD	]		]		1D X	X	x	US	X	/
9E		RS	RS	DE	^		^		1E Y	V	v	EOT	V	:
9F	US		US	DF		-	-		1F Z	UNSHIFT		DLE	LTRS	
A0	SP		SP	E0 \					20)	THIN SPACE		-		
A1 ~		!	!	E1	a		a		21 -	3		/		
A2 s		"	"	E2 S	b		b		22 +	PF		S		
A3 t	#		#	E3 T		c	c		23 <	!		T		
A4 u		\$	\$	E4 U	d		d		24 =	ADD THIN SPACE		U		
A5 v	%		%	E5 V		e	e		25 >	EM SPACE		V		
A6 w	&		&	E6 W		f	f		26 #	8		W		
A7 x				E7 X	g		g		27 \$	7		X		
A8 y		(	(	E8 Y	h		h		28 *	V		Y		
A9 z	)		)	E9 Z		i	i		29 (	@		Z		
AA	*		*	EA		j	j		2A %	4		ESC		
AB		+	+	EB	k		k		2B :	BELL		.		
AC		.	.	EC		l	l		2C ?			%		
AD		-	-	ED	m		m		2D !			ENQ		
AE		.	.	EE	n		n		2E .	EN SPACE		ETX		
AF	/		/	EF		o	o		2F @	QR		HT		
B0		0	0	F0 0	p		p		30 0	5		0		
B1	1		1	F1 1		q	q		31 1	(		1		
B2	2		2	F2 2		r	r		32 2	V RULE		2		
B3		3	3	F3 3	s		s		33 3	2		3		
B4	4		4	F4 4		t	t		34 4	EM LEADER		4		
B5		5	5	F5 5	u		u		35 5	6		5		
B6		6	6	F6 6	v		v		36 6	?		6		
B7	7		7	F7 7		w	w		37 7	EN LEADER		7		
B8	8		8	F8 8		x	x		38 8	&		8		
B9		9	9	F9 9	y		y		39 9	UPPER RAIL		9		
BA		:	:	FA	z		z		3A '	:		SYN		
BB	:		:	FB		{	{		3B ;	LOWER RAIL		#		
BC		<	<	FC					3C /			@		
BD	=		=	FD		~	~		3D .	1		NAK		
BE	>		>	FE		?	?		3E FF	QUAD CENTER		EM		
BF		?	?	FF	DEL		DEL		3F CR	RUBOUT		DEL		



TP-107-7-75

UNIVERSAL CODE CHART FOR DATA COMMUNICATIONS

8-BIT ASCII	7-BIT ASCII	EVEN PARITY ASCII	ODD PARITY ASCII	EBCDIC	6-BIT TRANSCODE	6-BIT TYPESETTER	EBCD	SELECTRIC	FIELD DATA	BAUDOT
BINARY	BINARY	BINARY	BINARY	BINARY	BINARY	BINARY	BINARY	HEX	BINARY	BINARY
HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX
A 11000001	01000001	01000001	11000001	A 11000001	00000001	00000001	A 11000001	23 A	00011001	00011001
B 11000010	01000010	01000010	11000010	B 11000010	00000010	00000010	B 11000010	13 B	00011010	00011010
C 11000011	01000011	01000011	11000011	C 11000011	00000011	00000011	C 11000011	73 C	00011011	00011011
D 11000100	01000100	01000100	11000100	D 11000100	00000100	00000100	D 11000100	08 D	00010100	00010100
E 11000101	01000101	01000101	11000101	E 11000101	00000101	00000101	E 11000101	08 E	00010101	00010101
F 11000110	01000110	01000110	11000110	F 11000110	00000110	00000110	F 11000110	58 F	00010110	00010110
G 11000111	01000111	01000111	11000111	G 11000111	00000111	00000111	G 11000111	58 G	00010111	00010111
H 11001000	01001000	01001000	11001000	H 11001000	00010000	00010000	H 11001000	07 H	00011000	00011000
I 11001001	01001001	01001001	11001001	I 11001001	00010001	00010001	I 11001001	07 I	00011001	00011001
J 11001010	01001010	01001010	11001010	J 11001010	00010010	00010010	J 11001010	61 J	00011010	00011010
K 11001011	01001011	01001011	11001011	K 11001011	00010011	00010011	K 11001011	61 K	00011011	00011011
L 11001100	01001100	01001100	11001100	L 11001100	00010100	00010100	L 11001100	51 L	00010100	00010100
M 11001101	01001101	01001101	11001101	M 11001101	00010101	00010101	M 11001101	51 M	00010101	00010101
N 11001110	01001110	01001110	11001110	N 11001110	00010110	00010110	N 11001110	51 N	00010110	00010110
O 11001111	01001111	01001111	11001111	O 11001111	00010111	00010111	O 11001111	51 O	00010111	00010111
P 11010000	01010000	01010000	11010000	P 11010000	00010000	00010000	P 11010000	29 P	00010000	00010000
Q 11010001	01010001	01010001	11010001	Q 11010001	00010001	00010001	Q 11010001	29 Q	00010001	00010001
R 11010010	01010010	01010010	11010010	R 11010010	00010010	00010010	R 11010010	29 R	00010010	00010010
S 11010011	01010011	01010011	11010011	S 11010011	00010011	00010011	S 11010011	29 S	00010011	00010011
T 11010100	01010100	01010100	11010100	T 11010100	00010100	00010100	T 11010100	52 T	00010100	00010100
U 11010101	01010101	01010101	11010101	U 11010101	00010101	00010101	U 11010101	52 U	00010101	00010101
V 11010110	01010110	01010110	11010110	V 11010110	00010110	00010110	V 11010110	52 V	00010110	00010110
W 11010111	01010111	01010111	11010111	W 11010111	00010111	00010111	W 11010111	52 W	00010111	00010111
X 11011000	01011000	01011000	11011000	X 11011000	00011000	00011000	X 11011000	7A X	00011000	00011000
Y 11011001	01011001	01011001	11011001	Y 11011001	00011001	00011001	Y 11011001	7A Y	00011001	00011001
Z 11011010	01011010	01011010	11011010	Z 11011010	00011010	00011010	Z 11011010	26 Z	00011010	00011010
a 11000001	01000001	01000001	11000001	a 11000001	00000001	00000001	a 11000001	23 A	00011001	00011001
b 11000010	01000010	01000010	11000010	b 11000010	00000010	00000010	b 11000010	13 B	00011010	00011010
c 11000011	01000011	01000011	11000011	c 11000011	00000011	00000011	c 11000011	73 C	00011011	00011011
d 11000100	01000100	01000100	11000100	d 11000100	00000100	00000100	d 11000100	08 D	00010100	00010100
e 11000101	01000101	01000101	11000101	e 11000101	00000101	00000101	e 11000101	08 E	00010101	00010101
f 11000110	01000110	01000110	11000110	f 11000110	00000110	00000110	f 11000110	58 F	00010110	00010110
g 11000111	01000111	01000111	11000111	g 11000111	00000111	00000111	g 11000111	58 G	00010111	00010111
h 11001000	01001000	01001000	11001000	h 11001000	00010000	00010000	h 11001000	07 H	00011000	00011000
i 11001001	01001001	01001001	11001001	i 11001001	00010001	00010001	i 11001001	07 I	00011001	00011001
j 11001010	01001010	01001010	11001010	j 11001010	00010010	00010010	j 11001010	61 J	00011010	00011010
k 11001011	01001011	01001011	11001011	k 11001011	00010011	00010011	k 11001011	61 K	00011011	00011011
l 11001100	01001100	01001100	11001100	l 11001100	00010100	00010100	l 11001100	51 L	00010100	00010100
m 11001101	01001101	01001101	11001101	m 11001101	00010101	00010101	m 11001101	51 M	00010101	00010101
n 11001110	01001110	01001110	11001110	n 11001110	00010110	00010110	n 11001110	51 N	00010110	00010110
o 11001111	01001111	01001111	11001111	o 11001111	00010111	00010111	o 11001111	51 O	00010111	00010111
p 11010000	01010000	01010000	11010000	p 11010000	00010000	00010000	p 11010000	29 P	00010000	00010000
q 11010001	01010001	01010001	11010001	q 11010001	00010001	00010001	q 11010001	29 Q	00010001	00010001
r 11010010	01010010	01010010	11010010	r 11010010	00010010	00010010	r 11010010	29 R	00010010	00010010
s 11010011	01010011	01010011	11010011	s 11010011	00010011	00010011	s 11010011	29 S	00010011	00010011
t 11010100	01010100	01010100	11010100	t 11010100	00010100	00010100	t 11010100	52 T	00010100	00010100
u 11010101	01010101	01010101	11010101	u 11010101	00010101	00010101	u 11010101	52 U	00010101	00010101
v 11010110	01010110	01010110	11010110	v 11010110	00010110	00010110	v 11010110	52 V	00010110	00010110
w 11010111	01010111	01010111	11010111	w 11010111	00010111	00010111	w 11010111	52 W	00010111	00010111
x 11011000	01011000	01011000	11011000	x 11011000	00011000	00011000	x 11011000	7A X	00011000	00011000
y 11011001	01011001	01011001	11011001	y 11011001	00011001	00011001	y 11011001	7A Y	00011001	00011001
z 11011010	01011010	01011010	11011010	z 11011010	00011010	00011010	z 11011010	26 Z	00011010	00011010
0 11010000	01010000	01010000	11010000	0 11010000	00010000	00010000	0 11010000	23 A	00011001	00011001
1 11010001	01010001	01010001	11010001	1 11010001	00010001	00010001	1 11010001	13 B	00011010	00011010
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3 11010011	01010011	01010011	11010011	3 11010011	00010011	00010011	3 11010011	08 D	00010100	00010100
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6 11010110	01010110	01010110	11010110	6 11010110	00010110	00010110	6 11010110	58 G	00010111	00010111
7 11010111	01010111	01010111	11010111	7 11010111	00010111	00010111	7 11010111	07 H	00011000	00011000
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9 11011001	01011001	01011001	11011001	9 11011001	00011001	00011001	9 11011001	61 J	00011010	00011010
A 11011010	01011010	01011010	11011010	A 11011010	00011010	00011010	A 11011010	61 K	00011011	00011011
B 11011011	01011011	01011011	11011011	B 11011011	00011011	00011011	B 11011011	51 L	00010100	00010100
C 11010000	01010000	01010000	11010000	C 11010000	00010000	00010000	C 11010000	51 M	00010000	00010000
D 11010001	01010001	01010001	11010001	D 11010001	00010001	00010001	D 11010001	51 N	00010001	00010001
E 11010010	01010010	01010010	11010010	E 11010010	00010010	00010010	E 11010010	51 O	00010010	00010010
F 11010011	01010011	01010011	11010011	F 11010011	00010011	00010011	F 11010011	51 P	00010011	00010011
G 11010100	01010100	01010100	11010100	G 11010100	00010100	00010100	G 11010100	29 Q	00010000	00010000
H 11010101	01010101	01010101	11010101	H 11010101	00010101	00010101	H 11010101	29 R	00010001	00010001
I 11010110	01010110	01010110	11010110	I 11010110	00010110	00010110	I 11010110	29 S	00010010	00010010
J 11010111	01010111	01010111	11010111	J 11010111	00010111	00010111	J 11010111	29 T	00010011	00010011
K 11011000	01011000	01011000	11011000	K 11011000	00011000	00011000	K 11011000	52 U	00010100	00010100
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M 11011010	01011010	01011010	11011010	M 11011010	00011010	00011010	M 11011010	52 W	00010110	00010110
N 11011011	01011011	01011011	11011011	N 11011011	00011011	00011011	N 11011011	52 X	00010111	00010111
O 11011100	01011100	01011100	11011100	O 11011100	00011100	00011100	O 11011100	7A Y	00011000	00011000
P 11011101	01011101	01011101	11011101	P 11011101	00011101	00011101	P 11011101	7A Z	00011001	00011001
Q 11011110	01011110	01011110	11011110	Q 11011110	00011110	00011110	Q 11011110	26 Z	00011010	00011010
R 11011111	01011111	01011111	11011111	R 11011111	00011111	00011111	R 11011111	26 Z	00011011	00011011
S 11010000	01010000	01010000	11010000	S 11010000	00010000	00010000	S 11010000	23 A	00011001	00011001
T 11010001	01010001	01010001	11010001	T 11010001	00					

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